THE UNIVERSITY OF QUEENSLAND

AUSTRALIA

Ternary oxide substrates for high-Q superconducting coplanar waveguide microwave resonators

Zachary Degnan

Under the supervision of
Dr. Peter Jacobson

A thesis submitted to the University of Queensland
in partial fulfilment of the degree of Bachelor of Science with Honours
School of Mathematics and Physics
June 2021

Typeset in LaTeX 2_ε.

The work presented in this Thesis is, to the best of my knowledge and belief original, except as acknowledged in the text, and has not been submitted either in whole or in part, for a degree at this or any other university.

Zachary Degnan

Abstract

As the field of quantum computing progresses, both the scale and complexity of qubit networks increase. With this, the threshold for acceptable losses in any single circuit component is reduced. Whilst progress has been made in reducing losses in superconducting hardware, further improvements are required for the realisation of more powerful quantum systems. Currently, device performance in the operational regime is limited by losses due to so called *two-level systems* (TLS) [1]. As both qubits and resonators can be made with the same materials and fabrication techniques, a high-Q resonator suggests that an equivalent qubit would be high performing. In this study we fabricate, characterise and measure high Q-factor superconducting CPW resonators on low-loss dielectric ternary oxide substrates, $MgAl_2O_4$ (MAO) and $LaAlO_3$ (LAO). Both devices use Al as the material for the superconducting film. The devices were characterised with atomic force microscopy (AFM), X-ray photoelectron spectroscopy (XPS) and X-ray reflectometry (XRR) during substrate treatment and after film deposition. In the single photon regime and at millikelvin temperature, we measured internal Q-factors of $Q_i = 9.9 \times 10^4$ for MAO and $Q_i = 9.9 \times 10^4$ for LAO. Both the LAO and MAO resonators were found to outperform an equivalent Al on Si resonator fabricated under the same conditions.

Acknowledgements

I would like to thank my supervisor, Peter, for his seemingly endless insights into the (nano)world of materials and surfaces, and for his encouragement throughout the project.

A huge thanks also goes out to the members of SQD Lab, who I would not have been able to complete my fabrications and measurements without. Thanks to Dr. Eric He for lending his time and expertise in nanofabrication to assist with lithography, etching and device measurement. Without Eric, this project would not have had the success it did! Thanks to Rohit Navarathna for wire-bonding my two chips, and for showing me how to operate the PLASSYS E-beam evaporator. Thanks to Dr. Eugene Sachkou for his assistance with dicing, which is not an easy process for uncommon materials such as LAO and MAO. Thanks to Alejandro Gómez Frieiro for giving me a run-down of the measurement setup in the SQD Lab, and for helping out with varying programming queries I had along the way. Finally, thanks to Assoc. Prof. Arkady Federov for allowing me to measure my devices in his lab's cryostat, and for the meaningful conversations along the way.

I would also like to acknowledge the support from my parents Sandie and Bernie, my sister Bec, my partner Bella, and my close friends. Thanks for always hearing me with open ears, whether I was excited or exhausted. Without these incredible people, I may never have finished this project - a million thanks.

Contents

List of Figures

List of Tables

List of Terms

The following lists are neither exhaustive nor exclusive, but may be helpful.

Abbreviations

Qubit	Quantum bit
TLS	Two-level system
SC	Superconducting
CPW	Coplanar waveguide
SCPW	Superconducting coplanar waveguide
TL	Transmission line
HV	High vacuum
PCB	Printed circuit board
cQED	Circuit quantum electrodynamics
AFM	Atomic force microscopy
XPS	X-ray photoelectron spectroscopy
XRR	X-ray reflectometry
XRD	X-ray diffraction
MA	Metal-air (interface)
SA	Substrate-air (interface)
SM	Substrate-metal (interface)
VNA	Vector network analyser
SD	Small dilution (fridge)
EBPVD	Electron-beam physical vapour deposition

Symbols

Q	Quality factor (Q-factor)
Q_l	Loaded Q-factor
Q_i	Internal Q-factor
Q_c	Coupling Q-factor
$\tan\delta$	Dielectric loss tangent
T_1	Qubit relaxation time
T_2	Qubit decoherence time
$\langle n_{ph} \rangle$	Average photon count
P_{app}	Applied power
p	Pressure
a	Primitive lattice constant

Materials [material type]

TMO	Ternary metal oxide (with general formula $A_xB_yO_z$)
Al	Aluminium [SC]
Nb	Niobium [SC]
Re	Rhenium [SC]
Pb	Lead [SC]
Ta	Tantalum [SC]
NbN	Niobium nitride [SC]
TiN	Titanium nitride [SC]
MAO	Magnesium aluminate ($MgAl_2O_4$) [insulator]
LAO	Lanthanum aluminate ($LaAlO_3$) [insulator]
MgO	Magnesium oxide [insulator]
GaAs	Gallium arsenide [semiconductor]
Si	Silicon [semiconductor]
STO	Strontium titanate ($SrTiO_3$) [semiconductor]

1 Introduction

1.1 Motivation

A programmable quantum computer with a mere 50 to 100 logical quantum bits (qubits) could outperform the most advanced classical computers of the current day. This achievement would have huge scientific implications in a number of fields including, but not limited to, chemistry, medicine, energy, material science and computer science [24]. Qubit networks of this scale are fundamentally limited by single-qubit coherence times, the time a quantum bit can store the amplitude and phase of a given quantum state [6]. Superconductivity provides one of the most appealing platforms for tackling the challenge of improving coherence time in scalable quantum computers [1, 21, 25]. Superconducting (SC) qubits are the only qubit systems to have demonstrated two-qubit fidelities, meaning that the physical qubit state corresponds well (above 90% fidelity) with the logical state of the qubit system [26]. Furthermore, the energy levels of superconducting qubits are tunable, whereas other proposed qubits, such as trapped ion qubits, are restricted to the energy structure determined by the atomic system [27]. In superconducting circuits, qubits can act as artificial two-level atoms with tunable energy levels [28]. Qubits operate in the single-photon quantum regime, leaving the delicate nature of quantum coherence easily disturbed by a number of effects present in superconducting (SC) technology [29]. Losses due to material defects, in particular atomic scale two level systems (TLS), are the fundamental limiting factor to quantum coherence in SC components such as resonators, capacitors, inductors and Josephson junctions (JJs) [2, 30–32]. The search for highly-ordered, defect-free superconducting films on semiconductor substrates has attracted increased interest in recent years [33].

As the field of quantum computing progresses, both the scale and complexity of qubit networks increase. With this, the threshold for acceptable losses in any single circuit component is reduced. Therefore, whilst progress has been made in reducing losses in SC hardware, further improvements are required for the realisation of more powerful quantum systems. In

an attempt to sidestep around various material loss mechanisms, research groups have designed three-dimensional resonator and qubit architectures. These qubits show promising coherence times on the order of (30 - 140 μs) [34, 35], however they are not suitable for large scale chip-based quantum computers due to their size. This step requires planar qubit architecture, which will be the focus of this report.

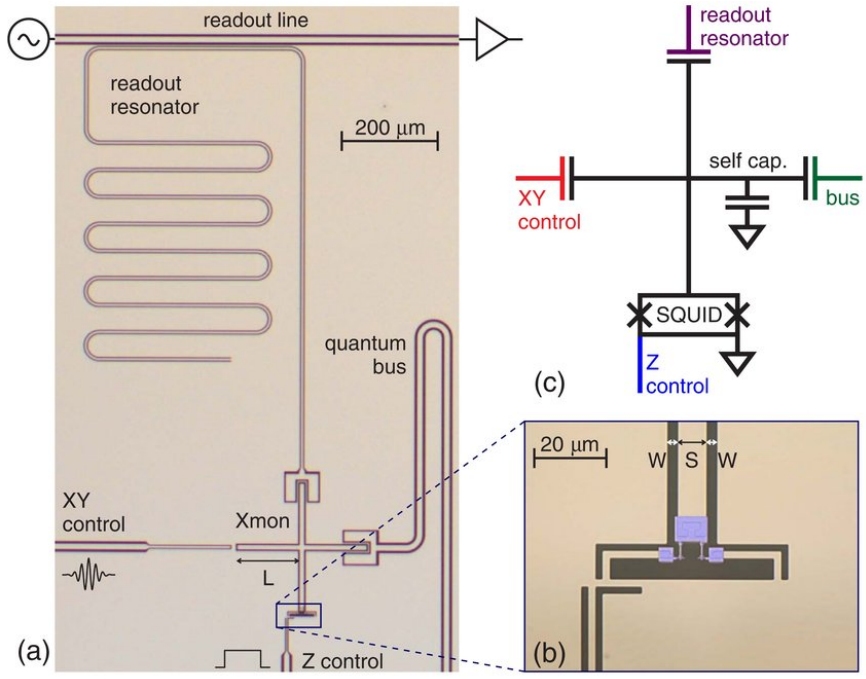


FIGURE 1.1: **a)** Example layout for a planar Xmon qubit. The the light-brown colour represents the metal SC film and dark-brown represents substrate exposed by lithography. The qubit is capacitively coupled to a readout $\lambda/4$ SCPW resonator, identical to the form of resonator studied in this report. Various other components of the Xmon qubit are labelled, however are not directly relevant to our discussion of resonators. **b)** The width S of the centre line (conductor) and dielectric insulating gap W of a capacitor. We will use S and W throughout this report, commonly referring to the central width and gap of a resonator and/or transmission line (TL). **c)** The qubit's electrical circuit. Figure taken from Ref. [2].

Superconducting coplanar waveguide (SCPW) [36] microwave (MW) resonators are central components in many planar qubit architectures, such as the Xmon qubit shown in Fig. 1.1 [2]. The Xmon qubit is a variation on the transmon qubit, which is a superconducting charge qubit that was designed to have reduced sensitivity to charge noise [37]. Furthermore, they have proven to be a vital tool for probing the nature and origin of decoherence mechanisms [30] and for measuring bulk dielectric properties of substrates in the low temperature and low power regime [38, 39]. Both qubits and resonators can be made with the same initial fabrication steps and materials. Therefore, a high quality factor (Q-factor) resonator suggests a long relaxation rate T_1 of a qubit (a primary measure for the quality of a qubit) made with the same materials and processes [6, 40]. This allows SCPW resonators, which generally have a less complex design than qubits, to be used as a stand-alone test-bed for

characterising material losses in the single-photon regime [30], and developing fabrication techniques that can then be applied directly to planar SC qubits [29].

The internal (or intrinsic) Q-factor (quality factor) Q_i at low temperature, $T \sim 10$ mK, and single-photon excitation power, $\langle n_{ph} \rangle \sim 1$ (in the operational regime for SC qubits) is critical in experimentally measuring the quality of a SCPW microwave resonator [41]. A higher Q_i corresponds to a resonator with fewer internal losses and sharper microwave resonance. The dielectric loss tangent $\tan\delta$ can be extrapolated from experimental measurements of Q_i, allowing for direct characterisation of dielectric losses due to TLS [40, 42].

Superconducting planar circuits such as qubits and resonators are comprised of dielectric (semiconducting and insulating) substrates (typically sapphire (Al_2O_3) or silicon (Si)) upon which superconducting thin metal films (most commonly aluminium (Al) or niobium (Nb)) are deposited and patterned. It has become clear that the vast majority of TLS reside in thin amorphous oxide films at the interfaces - substrate-metal (SM), substrate-air (vacuum) (SA) and metal-air (vacuum) (MA) - rather than in the bulk of materials [1, 43, 44]. These TLS act as 'unwanted qubits' [40] interfering resonantly with the targeted qubit computational states [32]. This result emphasises the importance of carefully designed devices with atomically accurate interfaces; a resonator with oxide-free interfaces will have a reduced number of parasitic TLS and therefore a higher Q_i than an identical resonator with interface oxides. Therefore, various strategies have been employed to reduce TLS in devices. Over the past decade, studies have analysed the Q_i of resonators as a function of geometry and scale [2, 41, 43–47], material [29, 41, 45, 47–50] and fabrication technique [40, 45, 51–54]. All of these approaches share the over-arching goal of minimizing TLS losses to create a high quality resonator in the operating regime for SC qubits.

One of the most common material platforms for CPW resonator fabrication consists of a thin Al film on a Si substrate (Al on Si) [6, 40, 45, 51, 52, 54]. Silicon is a desirable substrate choice due to its compatibility with classical integrated circuit (IC) technology and availability, well characterised surface treatment processes and ease of fabrication [6, 40, 55, 56]. Another popular substrate choice is sapphire; it is known to have a low dielectric loss tangent, high chemical inertness and has well-known surface treatments allowing for reproducible high-quality fabrication [53, 57–60]. Al has become the most popular material choice for the superconductor due to its availability, thermal stability [61] and self-limiting native oxide growth [52]. Previous research has also explored the effectiveness of non-standard dielectric-superconductor combinations that are suitable for epitaxial film growth in the context of quantum computing applications with varying degrees of success. In particular, gallium arsenide (GaAs) [33, 61, 62], indium antimonide (InSb) [63] and magnesium dioxide (MgO) [39, 64–66] have been employed as alternate substrates. Whilst devices have been fabricated with non-standard substrates there is still limited characterisation data in the low power and low temperature limits, where TLS losses become prominent [65]. Therefore, there is still much more work to be done in the search for the most suitable substrates for SC film growth and operation in the quantum regime. For any choice of material platform the fabrication process must be carefully designed to minimise chemical or thermal damage to materials during fabrication, minimise oxide growth, reduce surface roughness and facilitate near-epitaxial film growth. Therefore, the process of choosing a new material platform necessitates the need for an updated fabrication procedure.

In general, substrates for superconducting films should be crystalline semiconductors or insulators with a low dielectric loss tangent at low power and temperature. This minimises dielectric losses in the bulk of the material, and ensures that the majority of TLS are confined to native oxides and other material defects and inhomogeneities at interfaces. A device fabricated with a lossy dielectric substrate will not have a high Q_i and is not suitable for quantum circuitry. Conventional high temperature measurements of dielectric losses do not necessarily coincide with low temperature and power values [32]. Furthermore, the choice of substrate should be informed by the superconductor material and vice-versa. Since substrates are single-crystals, with a known lattice constant corresponding to the size of the unit crystal cell, they should be chosen to match within a reasonable threshold to the lattice constant of the film. This minimises strains at the SM interface and allows films to grow more uniformly [67], creating a SC film with fewer surface defects.

In this study, we fabricate and operationally test Al CPW resonators on $LaAlO_3(100)$, $MgAl_2O_4(100)$ and Si(100) substrates, where the (100) corresponds to the Miller indices along the direction in which the crystal is cut by the manufacturer (MTI Crystals). We will hereafter refer to the materials as LAO and MAO respectively. These substrates were chosen due to their low dielectric losses and high dielectric constant, high thermal and chemical stability and, in the case of MAO, a well-matched lattice constant with (poly)crystalline Al [68–74]. Furthermore, the LAO crystal has structural similarities with high-T_C superconductors such as $SrTiO_3$ (STO), making it an appealing substrate for applications in high-T_C superconducting devices [75–77]. We have chosen to use exclusively Al films to allow for direct comparison of our results with resonators made on standard substrates with Al films.

1.2 A brief historical overview on high-Q CPW resonators

SCPW resonator quality has improved drastically over the last decade of research. Prior to 2012, state-of-the-art CPW resonators could only reach internal Q-factors above 1 million at high excitation powers [46, 78], outside of a qubit's operational regime. In 2012, the first resonators with $Q_i > 10^6$ were fabricated and measured in the single-photon regime at UC Santa Barbara [53]. The group produced a number of these $\lambda/4$ Al on sapphire resonators, exploring the effectiveness of various chemical and physical substrate surface treatments on otherwise identical devices. Their best resonator had a low power Q_i of 1.72×10^6, whilst the worst had $Q_i = 0.16 \times 10^6$. These results conclusively showed the importance of fabrication procedure on resonator quality.

Eight years later, in 2020, a collaboration between UC Berkeley and the Lawrence Berkeley National Laboratory produced Nb-on-Si SCPW resonators with median Q_i of 5.3×10^6 [30]. The group claims to have achieved these record Q_i values by removal of interfacial oxides, resulting in chips with atomically perfect SM interfaces. Through selective etching they were able to analyse the source and nature of TLS losses, concluding that 70% arise from Si oxides and at least 15% from Nb oxides. This study gives further credence to the now-accepted theory that TLS losses can be greatly reduced through removal of native surface oxides and preparation of atomically-perfect interfaces. Furthermore, the study

demonstrates that any well-engineered material system can be effective for use in SCPW resonators. At this time, a number of research groups are able to robustly produce CPW resonators with Q-factors above 1 million including the aforementioned and studies in references [48, 52, 54, 79].

When comparing measurements of Q_i across resonators, it is important to acknowledge the effect of scale on quality factor. A resonator with larger dimensions (i.e. larger gap S and width W as seen in Fig. 1.1) will have a higher electric field to surface area ratio (filling factor), and will therefore be less impacted by surface losses due to TLS [2, 22, 40]. Therefore, it is not useful to directly compare the quality factor of two resonators fabricated at different scales, i.e. with conductor widths of 10μm and 20μm. The extent to which a chip is scaled should take into consideration the scalability of the design (recall that at least 50 qubits were required to demonstrate quantum supremacy [24]).

2 Background

2.1 Theoretical principles

Here, we provide the theoretical background required to understand the operational principles and measurement of SCPW microwave resonators. This includes brief theoretical descriptions of the dielectric constant ϵ and loss tangent $\tan\delta$ [80, 81], superconductivity [82], internal Q-factors [15, 83] and TLS theory [84].

2.1.1 Maxwell's equations and the dielectric loss tangent

Maxwell's equations [80] provide a dynamical mathematical description of free and interacting electromagnetic fields. Considering the electromagnetic field in the presence of charge and current density, ρ and $\mathbf{J}$ respectively, Maxwell's equations are written as [81]

$$\nabla \cdot \mathbf{D}(\mathbf{r},t) = 4\pi\rho(\mathbf{r},t) \tag{2.1}$$

$$\nabla \cdot \mathbf{B}(\mathbf{r},t) = 0 \tag{2.2}$$

$$\nabla \times \mathbf{E}(\mathbf{r},t) = -\frac{1}{c}\partial_t \mathbf{B}(\mathbf{r},t) \tag{2.3}$$

$$\nabla \times \mathbf{H}(\mathbf{r},t) = \frac{4\pi}{c}\mathbf{J}(\mathbf{r},t) + \frac{1}{c}\partial_t \mathbf{D}(\mathbf{r},t), \tag{2.4}$$

where the electric field $\mathbf{E}$ is related to the electric displacement field by $\mathbf{D} = \epsilon\mathbf{E}$ and the magnetic field $\mathbf{H}$ to the magnetic flux density by $\mathbf{B} = \mu\mathbf{H}$. Here, $c = 2.998 \cdot 10^8 \mathrm{m\,s^{-1}}$ is the speed of light, ϵ is the dielectric constant and μ is the magnetic permeability, which is equal to vacuum magnetic permeability $\mu = \mu_0 = 1.2566 \cdot 10^{-6} \mathrm{H\,m^{-1}}$ [85] for non-magnetic materials. The relative permeability, defined as $\mu_r = \frac{\mu}{\mu_0}$, is therefore $\mu_r = 1$ for non-magnetic materials. Similarly, the relative permittivity of a dielectric is $\epsilon_r = \frac{\epsilon}{\epsilon_0}$, where $\epsilon_0 = 8.8542 \cdot 10^{-12} \mathrm{F\,m^{-1}}$ and $\epsilon_r \geq 1$ for dielectric materials (such as dielectric substrates) and $\epsilon_r = 1$ for vacuum [81].

Following the derivation given in Ref. [81], we assume a harmonic time dependence of the electric displacement field $\partial_t \mathbf{D} = -i\omega\mathbf{D}$ of frequency ω, and employ Ohm's law $\mathbf{J} = \sigma\mathbf{E}$, where σ is the conductivity. Now, equation 2.4 can be rewritten as

$$\nabla \times \mathbf{H}(\mathbf{r}, t) = \frac{1}{c}(4\pi\sigma - i\omega\epsilon)\mathbf{E} = -\frac{i\omega}{c}\hat{\epsilon}\mathbf{E}. \tag{2.5}$$

Here, the hat $\hat{}$ represents the complex dielectric constant

$$\hat{\epsilon} = \epsilon + i\frac{4\pi\sigma}{\omega} = \epsilon_1 + i\epsilon_2. \tag{2.6}$$

The real part of the complex dielectric constant, ϵ_1, describes lossless dispersion, whilst the imaginary part $\epsilon_2 = \frac{4\pi\sigma}{\omega}$ describes lossy absorption. Since $\mathbf{D} = \hat{\epsilon}\mathbf{E}$, it can be seen that the complex dielectric constant conveniently describes the phase and amplitude between the electric field $\mathbf{E}$ and displacement $\mathbf{D}$.

In capacitors (such as those found coupling a CPW resonator to a TL), energy is lost due to absorption in the dielectric (substrate). Conventionally, the extent of dielectric loss for a material with a complex dielectric constant $\hat{\epsilon}$ is given by the dielectric loss tangent [32]

$$\tan\delta = \frac{\epsilon_1}{\epsilon_2} \equiv \frac{\mathrm{Re}(\hat{\epsilon})}{\mathrm{Im}(\hat{\epsilon})}. \tag{2.7}$$

The number of coherent oscillations in a resonator is inversely related to the amount of energy dissipation; a larger δ corresponds to a lossier resonator with a lower number of coherent oscillations. Since the Q-factor describes the extent of resonance, we can relate Q and δ by $Q \sim 1/\delta$ [32].

2.1.2 Coplanar waveguide $\lambda/4$ resonators

Coplanar waveguide (CPW) resonators were initially proposed in 1969 by C. Wen [36] as a way to simplify microwave circuits, in particular radar and communication systems. The first CPW resonator fabricated by Wen yielded $Q = 173$ at 4 GHz. In contrast to earlier microwave circuit designs, all conducting elements, including ground planes, are fabricated on one side of a single dielectric substrate (hence the name coplanar). This allows for simpler fabrication processes, easier connectivity to other circuit elements and more freedom in the choice of substrate material and dimension [36]. CPW resonators can be directly patterned into a conducting layer on top of a dielectric substrate by lithography; only one layer of material has to be deposited normal to the substrate, and lithography is only required on this layer [83]. This fabrication process is much simpler than that of many other circuit quantum electrodynamics (cQED) components, such as Josephson Junctions used in transmon qubits, which require multiple depositions at varying angle and lithographic steps, as well as careful alignment of layers [86].

A typical design for a $\lambda/4$ resonator coupled capacitively to a transmission line (TL) is shown in figure 2.1. A $\lambda/4$ resonator is characterised by a waveguide with one shorted end and one open end. The boundary conditions in this configuration necessitate that the electric field is zero at the shorted end, and maximum at the open end, so the fundamental

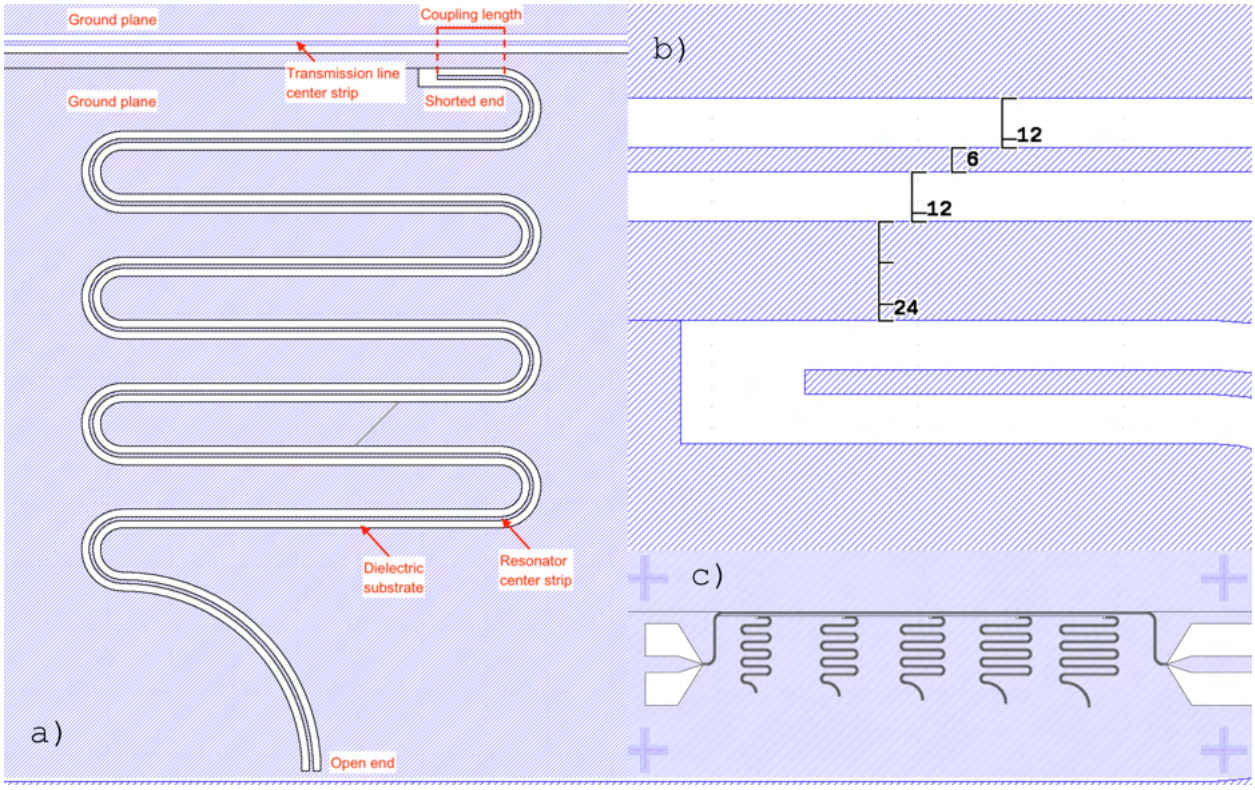


Figure 2.1: **a)** $\lambda/4$ CPW resonator capacitively coupled to a transmission line (TL), patterned on top of a dielectric substrate. Blue represents the SC metal layer (Al), and white represents the dielectric substrate (LAO or MAO in our case). The horizontal line along the top is the TL, and the meander extending to the bottom of the image is the $\lambda/4$ resonator. The shorted end of the resonator is coupled to the TL for a length denoted coupling length, the length where the resonator runs parallel to the TL. The other end of the resonator is open, defining the structure as a $\lambda/4$ resonator. The central conducting strips of the resonator and TL are bounded by a parallel strip of the dielectric substrate. The rest of the metal plane is grounded. **b)** This image shows the coupling length between TL and resonator in detail with labelled lengths for resonator/TL gap and width (units of µm). For this particular resonator the width $S = 6$µm and gap $W = 12$µm. The distance between the TL and resonator (24µm here), and the coupling length determines the coupling strength between the TL and resonator. **c)** A complete CPW resonator chip. Pads on the left and right of the chip are used for bonding to an external printed circuit board (PCB). There are five $\lambda/4$ resonators of varying microwave frequency coupled to a single TL. The crosses are used as dicing marks. Images taken from the resonator designed for patterning on the LAO substrate in this project, made on klayout using Python code adapted from Eric He (SQD Lab at UQ).

mode has a wavelength λ that is four times the total length L of the resonator [87]. The electric field distribution for the first, third and fifth standing wave modes on a $\lambda/4$ resonator is shown in figure 2.2. Employing a zeroth-order quasi-static approximation to estimate the phase velocity v_{ph} of a wave confined within a CPW resonator, we define the effective dielectric constant as the average between the substrate's relative permittivity ϵ_r and vacuum permittivity. Since SCPW resonators deal only with non-magnetic materials, we can set $\mu_0 = 1$. The relative permittivity of the vacuum is unity, so the phase velocity inside the TL

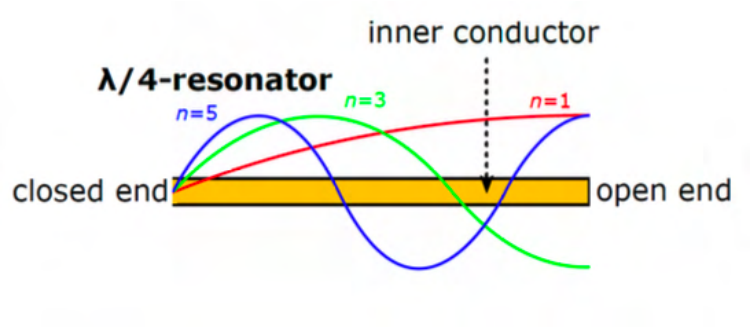


FIGURE 2.2: Electric field distribution for standing wave modes 1, 3 and 5 on a $\lambda/4$ resonator. Due to boundary conditions, the electric field strength is zero at the shorted (closed) end and maximum at the open end. Adapted figure taken from Ref. [3], originally from Ref. [4].

and resonator is given by [36]

$$v_{ph} = \frac{c}{\sqrt{\frac{\epsilon_r+1}{2}}} = \sqrt{\frac{2}{\epsilon_r+1}}c, \tag{2.8}$$

where we have assumed that the electromagnetic wave is travelling half in the substrate with permittivity ϵ_r, and half in vacuum. The resonance frequency can then be found by [15]

$$f_r^{(n)} = \frac{v_{ph}}{4L}(2n-1) = \frac{\sqrt{\frac{2}{\epsilon_r+1}}}{4L}c(2n-1), \tag{2.9}$$

where $n = 1, 2, 3, ...$ is the mode number and L is the resonator's total length (including coupling length). The frequency of the fundamental mode, which will be targetted for measurements of the resonator's Q-factor, is

$$f_r^{(1)} = \frac{\sqrt{\frac{2}{\epsilon_r+1}}}{4L}c. \tag{2.10}$$

2.1.3 Superconductivity

Superconducting materials have the unique properties of being a perfect conductor (a vanishing DC-resistance) and near-perfect diamagnet [88] (complete expulsion of any external magnetic field, known as the Meißner-Ochsenfeld effect) below the material's superconducting critical temperature T_C [82]. The accepted theoretical description of superconductivity, known as BCS-theory, was provided by Bardeen, Cooper and Schrieffer in 1957 [82]. In BCS-theory, electron pairs, called Cooper pairs, are formed due to an attractive force attributed to an electron-phonon interaction. In the superconducting regime, this attractive interaction dominates the short-range repulsive Coulomb force and Cooper pairs are formed [82]. A macroscopic description of electromagnetic fields in superconductors is given by the London equations [89], which predict a temperature dependent penetration depth $\lambda_L(T)$.

The penetration depth is given as [89]

$$\lambda_L(T) = \sqrt{\frac{m_e c^2}{4\pi e^2 n_s(T)}}, \tag{2.11}$$

where m_e and e are the mass and charge of SC charge carriers and $n_s(T)$ is their density. Near the critical temperature, T_C, the temperature dependence of penetration depth is given by the empirical law [90]

$$\lambda_L(T) = \frac{\lambda_L(T=0)}{\sqrt{1-\left(\frac{T}{T_C}\right)^4}}, \tag{2.12}$$

with

$$n_s(T) = n_s(T=0)\left(1-\left(\frac{T}{T_C}\right)^4\right). \tag{2.13}$$

In this study, we consider only Type I superconductors. Type I SCs have a critical magnetic flux density B_C. For an external magnetic flux density $B_{ext} < B_C$, the superconductor retains its diamagnetic properties and loses them when $B_{ext} > B_C$ [90]. In comparison to SC metals, normal metals have losses that lead to very low Qs [30, 36].

2.1.4 Internal quality factor Q_i

The Q-factor of a resonant circuit gives a measure of its loss. A resonator with a high-Q is able to store a large amount of energy with low losses [87]. The Q-factor that can be extracted directly from transmission measurements on the resonator corresponds to the total, or loaded Q-factor Q_l, which includes contributions from other conductors, the readout circuit, and external factors that do not come directly from the chip being tested, as well as contributions from the resonator itself [65]. External contributions are attributed to the coupling quality factor Q_c. The quality factor of the resonator itself (neglecting any coupling to external elements) is called the internal (or intrinsic) quality factor Q_i. The three quantities are related by [6]

$$\frac{1}{Q_l} = \frac{1}{Q_c} + \frac{1}{Q_i}. \tag{2.14}$$

Through the improvement of fabrication process and material choice, we hope to minimise TLS in SCPW resonators. TLS losses contribute to reduction in Q_i, so we are therefore aiming to improve Q_i exclusively. For a good readout signal, Q_c and Q_i should be similar [87]. If $Q_i >> Q_c$, $Q_i^{-1} << Q_c^{-1}$, so the coupling Q-factor will have a much larger impact on Q_l. This can be seen directly in equation 2.14, and must be considered during measurement.

2.1.5 S_{21} transmission signal measurement

The resonance of a transmission line (TL) coupled CPW resonator can be characterised by measurement of the S_{21} transmission response [5, 91]. This is a measure of the amount of

power transmitted along the feedline from input to output [92]. It is related to the applied and transmitted power (P_{app} and P_{trans} respectively) by [48]

$$|S_{21}|^2 = \frac{P_{trans}}{P_{app}}. \tag{2.15}$$

At a resonators' natural frequency $f_0 = \omega_0/2\pi$, the measure of S_{21} transmission exhibits a dip with the geometry of a notch filter, as seen in figure 2.4a. For a chip with multiple resonators of varying frequency coupled to a shared TL, the $|S_{21}|$ measurement would show an absorption dip at the natural frequency of each resonator. Absorption will also occur for higher harmonics, however we will only consider the fundamental resonance. The applied power P_{app} in dBm is related to the average photon number in the resonator as [48, 93]

$$\langle n_{ph} \rangle = \frac{\langle E_{int} \rangle}{\hbar\omega_0} = \frac{2}{\hbar\omega_0^2}\frac{Z_0}{Z_r}\frac{Q_l^2}{Q_c}P_{app}, \tag{2.16}$$

where Z_0 is the circuit's impedance ($Z_0 = 50\Omega$) and Z_r is the resonator impedance, which is normally designed to be as close to Z_0 as possible, in which case $\frac{Z_0}{Z_r} \to 1$. $\langle E_{int} \rangle$ is the average energy stored in the resonator, and Q_l is the loaded quality factor.

Fitting a model to the S_{21} transmission measurement

To fit our data, we employ the model for S_{21} notch measurements developed by Petersan and Anlage [94], and extended by Gao [95], Khalil et al. [92] and Probst et al. [5]. The model considers the transmission of a notch type resonator as a product of the transmission due to the (ideal) resonator, and the transmission due to contributions from the environment, where the environment is considered to be all signal contributions from outside the sample. Modern VNAs can measure complex signals, so the model therefore makes use of complex scattered data as opposed to real-valued quantities only. The complex transmission of an ideal notch resonator is given as [5, 92, 95]

$$S_{21}(f) = \underbrace{ae^{i\alpha}e^{-2\pi f\tau}}_{\text{environment}}\underbrace{\left[1 - \frac{(Q_l/|Q_c|)e^{i\phi}}{1 + 2iQ_l(f/f_0 - 1)}\right]}_{\text{ideal resonator}}. \tag{2.17}$$

This equation has two components; the *environmental* signal contribution is given in the part outside of the square brackets, and the contribution from an *ideal resonator* is given inside the square brackets. For the ideal resonator contribution, f is the probe frequency, f_0 is the natural resonance frequency of the resonator, and $|Q_c|$ is the magnitude of the (complex) coupling quality factor. The phase of the coupling quality factor, $e^{i\phi}$, accounts for asymmetries in the ideal resonator's transmission signal due to mismatched input and output impedances, which are quantified in the value of ϕ, or standing waves reflected between the input and output ports of the resonator's transmission line. The complex coupling quality factor is $Q_c = |Q_c|e^{i\phi}$ [92].

The *environmental* term accounts for attenuation (from circuit elements and cables) or amplification in the measurement circuit in the parameter a, which acts as an additional

amplitude correction. In a typical measurement setup, cables are used to carry signal from the source, to the sample, to the VNA for readout. There will therefore be some frequency-dependent phase change due to the length of the cables, the finite speed of light, and the transmission character (transfer function) of the lines. This change is referred to as cable delay, which is captured in the parameter τ. Finally, we allow for a phase offset α at the device, which is a consequence again of the cable length.

Figure 2.3 shows the normalised transmission according to equation 2.17 [5]. Figure 2.3a shows the resonance circle in complex plane, where $\Im\{S_{21}\}$ is parametrically plotted against $\Re\{S_{21}\}$. This type of plot gives information about the ratio of loaded and coupling quality factors, and the phase correction due to ϕ. The diameter of the resonance circle, as labelled with d in figure 2.3a, is $d = Q_l/|Q_c|$. A resonator coupled critically to the transmission line will have $d = 0.5$ [87], which is the condition for maximum power transfer. If $d < 0.5$, the resonator is said to be undercoupled to the feedline, and if $d > 0.5$, it is said to be overcoupled. For high-sensitivity applications such as ours, the resonators should be slightly undercoupled [15, 87]. On the parametric resonance plot, this would correspond to the resonance circle being *squeezed* perpendicular to the direction of d. The diameter of the circle perpendicular to d, which we will refer to as D, is related to the internal quality factor by $D = Q_i/Q_c^*$, where $Q_c^* \equiv (Z_0/|Z|)Q_c$ is the rescaled coupling quality factor [53]. Z_0 is the cable impedance, and $Z = |Z|e^{i\phi}$ is the complex impedance. The point shown as $f = f_r$ in figure 2.3a is equivalent to the point on-resonance (which we refer to as f_0) in figure 2.3b. The points ± 90 degrees around the circle from this point fall within the FWHM of the resonance dip shown in figure 2.3b, with a frequency difference $\Delta f_{3\text{dB}}$ [53].

A python implementation of the circle fit algorithm is available via Sebastian Probst's Github [23], the workings of which are thoroughly detailed in reference [5]. This python package was used throughout this study.

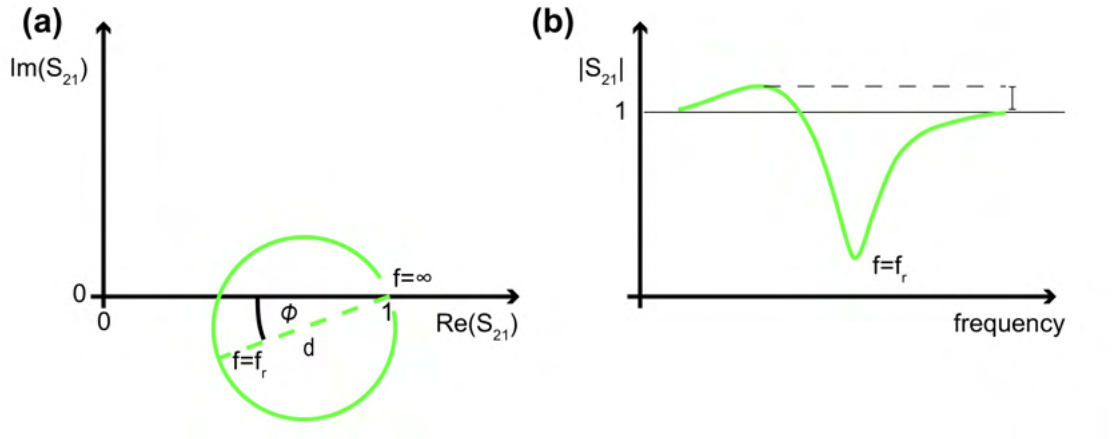


Figure 2.3: **a)** Parametric plot of the complex S_{21} transmission signal according to the model given in equation 2.17. **b)** Figure taken from Probst et al. [5].

The dependence of quality factor on photon number

Figure 2.4b) shows the S-shaped curve of internal Q-factor Q_i as a function of average photon number $\langle n_{ph} \rangle$. At low photon number Q_i decreases due to TLS losses, whilst at higher photon count the TLS may become saturated and other loss mechanisms dominate [46, 53, 96]. It is currently not known if TLS become saturated in the high-photon regime, or if their contribution to losses are simply negligible in this regime. By fitting excitation-power-dependent Q_i data to a TLS-based loss model, the TLS-specific loss tangent δ_{TLS} can be extracted. The TLS loss model, detailed in Ref. [5], is given as

$$\frac{1}{Q_i} = F\delta^0_{TLS} \frac{\tanh\left(\frac{\hbar\omega_0}{2k_BT}\right)}{\left(1+\left(\frac{\langle n_{ph}\rangle}{n_c}\right)\right)^{\beta}} + \delta_{other}, \tag{2.18}$$

where F is the filling factor, which is a ratio between the total electric field stored in the circuit's total volume, and the field stored in the TLS host volume (i.e. oxides on surfaces and interfaces). A smaller filling factor (corresponding to fewer surface oxides) will therefore produce a higher Q_i according to this model. The TLS loss tangent $\delta_{TLS} = 1/Q_{TLS}$ characterises the losses attributed directly to dissipation through TLS and n_c is the cavity photon number required to saturate a single TLS. δ_{other} describes all non-TLS losses, which dominate in the high-photon count regime. By fitting this model to experimental data, as shown in figure 2.4b), a value for $F\delta_{TLS}$ and δ_{other} can be extracted. Since we are concerned with device-specific improvements, we are not concerned with the improvement of δ_{other} (corresponding to Q_c). If the filling factor F can be estimated, for example by quantifying the volume of surface oxide, reasonable bounds on the TLS loss tangent δ_{TLS} could be extracted.

2.1.6 TLS theory: the standard tunnelling model

Two-level systems and their interactions are described by the standard tunnelling model, which we will give a brief overview of here. An extensive review of the standard tunnelling model and its implications is given by Esquinazi [84]. As the name implies, the standard tunnelling model assumes that an atom can tunnel between two energetically similar configurations, modelled as minima in a double-well potential as shown in figure 2.5. At high temperatures, an atom in either well could be shifted to the other by a thermal kick, however at sufficiently low temperatures this cannot happen and the dynamics are governed by quantum tunnelling between the wells. In this system, transitions can be driven by external fields, as in the case of parasitic TLS in CPW resonators. Depending on the magnitude of energy asymmetry ϵ between the wells, the eigenstates $|\psi_+\rangle$ and $|\psi_-\rangle$ could be described either as: a) the particle being classically located in either the left or right well; or b) an odd or even quantum superposition of the classical left and right states. The energy associated with a particle tunnelling across the energy barrier is Δ_0. We can describe this configuration in the position basis $(|L\rangle, |R\rangle)$ by the TLS Hamiltonian H_{TLS} given in matrix form as [1]

$$H_{TLS} = \frac{1}{2}\begin{pmatrix} \epsilon & \Delta_0 \\ \Delta_0 & -\epsilon \end{pmatrix}. \tag{2.19}$$

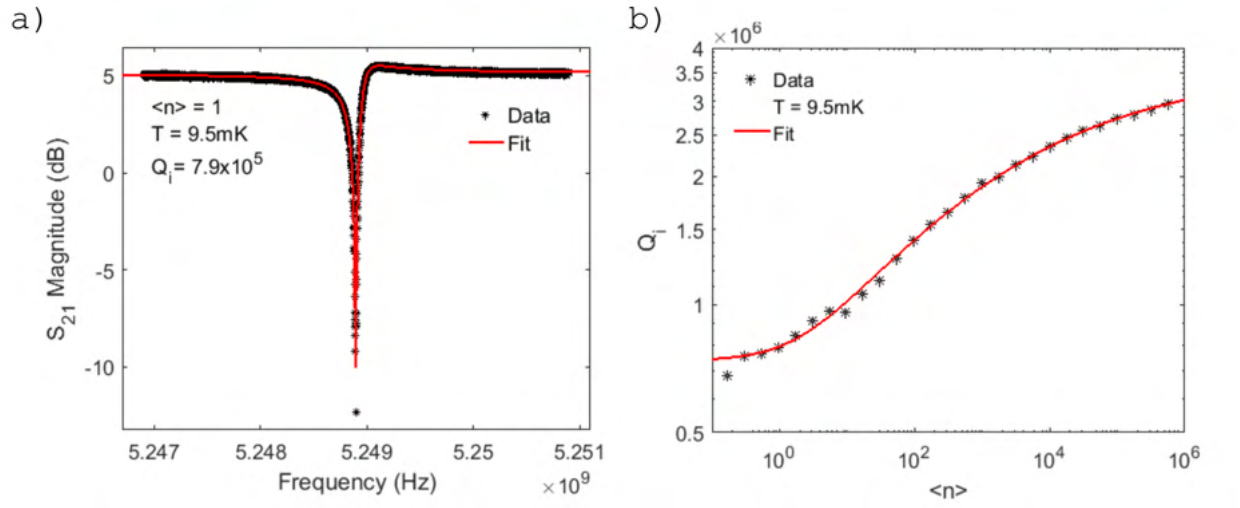


Figure 2.4: **a)** Black data-points show experimental $|S_{21}|$ values for a superconducting Al CPW resonator on a Si substrate. The fit [5] from which the resonator parameters (Q_i, Q_c, ω_0) are extracted is shown in red. The measurement was performed in the single photon regime, with an applied power of $P_{app} = -146$ dBm (which corresponds to $\langle n_{ph} \rangle = 1$) and at a temperature of 9.5 mK. The extracted resonator parameters are $f_0 = \omega_0/2\pi = 5.23$ GHz, $Q_c = 33 \times 10^3$ and $Q_i = 7.9 \times 10^5$. **b)** Plot of experimental data (black) of Q_i at varying cavity photon number for a SCPW resonator at 9.5 mK. The fit shown in red describes TLS losses as a function of $\langle n_{ph} \rangle$. Both figures a) and b) taken from Burnett et al. [6].

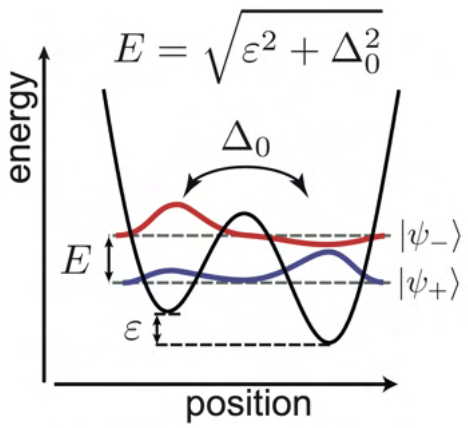


Figure 2.5: A double-well depiction of TLS described by the standard tunnelling model. The energy difference $E = \sqrt{\epsilon^2 + {\Delta_0}^2}$ between TLS eigenstates $|\psi_-\rangle$ and $|\psi_+\rangle$ is determined by the tunnelling energy Δ_0 and energy asymmetry ϵ between the two wells. Figure taken from Müller et al. [1].

Whilst figure 2.5 provides a useful intuitive picture of TLS, it does not tell us what TLS are (i.e. the charge and nature of the tunnelling particles, the form of the potential wells and the particle mass). The study of correlations between TLS-hosting amorphous surface oxides and Q-factors of SCPW resonators offers a promising route towards an understanding of the

microscopic origins of TLS [1, 79]. So far, such studies have suggested OH bonds and defects in aluminium oxides (AlO_x) and silicon oxides (SiO_2) as a potential origin of TLS [32, 97]. Experiments on TLS in SC circuits have shown that a distribution of TLS with eigenenergies in the range of circuit frequencies (generally 4-8 GHz) leads to dissipation of energy from the circuit into the TLS environment [98]. A recent study by Lisenfeld et al. [99] used a mechanical strain field to tune TLS energies, and experimentally measured a coherent TLS-TLS interaction in an amorphous oxide layer within a SC qubit. This study was designed under the assumption of the standard tunnelling model, and gives experimentally-backed credence to the theory.

Since TLS are created in a random manner by atoms in a solid, there is a large range of potential barrier heights, switching rates and eigenenergies in a TLS ensemble [1]. In 1981, it was shown by Dutta and Horn [100] that a distribution of TLS in a solid could produce the characteristic spectrum of low-frequency $1/f$ noise, however a direct link between a TLS ensemble and measured $1/f$ noise in the same device has not yet been made [1]. $1/f$ noise is found across a tremendous range of electric circuits and physical systems [100], and is a large contributor to decoherence in SC circuits [31, 101]. A microscopic understanding of the origins of TLS could be highly beneficial to noise reduction in a range of areas outside SC quantum computing.

2.2 Materials, fabrication and geometry of CPW resonators

Here, the choice of material combinations, fabrication protocols and chip geometry for SCPW resonators is discussed within the context of minimising TLS in these devices. Good material choices and fabrication procedures will allow for controlled removal of surface oxides at interfaces, defect-free surfaces and near-epitaxial defect-free film growth. The materials should also be thermally, chemically and temporally stable (i.e. show no degradation in quality over time), and ideally should not be extremely sensitive to external magnetic fields. SCPW resonator geometries, which will not be discussed at length here, should be designed with the following considerations: reduction of the TLS filling factor F; scalability of the design; ease of fabrication; and reduction of unwanted coupling between circuit elements and/or external elements.

2.2.1 Material choices and considerations

Superconducting materials

The conductors in SCPW resonators are commonly chosen to be aluminium (Al) or niobium (Nb), with more exotic choices being rhenium (Re) [47], titanium nitride [54], tantalum (Ta) [50, 102] and lead (Pb) [61]. The choice between Nb and Al depends on the exact type of device being made, and the conditions under which it will be operator. Nb has a higher critical temperature than Al (9.26 K and 1.20 K respectively [103]) and is also less sensitive to applied magnetic fields [104]. This would make Nb a more desirable choice in cQED systems that use applied magnetic fields for control, such as spin based qubits [105]. Al

has the advantage of being more accessible than Nb, and also has a lower melting point, allowing for simpler fabrication procedures than those required for Nb [61]. For this reason, in a system that does not require applied magnetic fields, Al is the more common choice. Pb superconductors have been shown to produce resonators with large magnetic tolerance, but suffer from degradation with age [61]. In 2020, Place et al. [50] produced Ta on sapphire transmon qubits with an average $T_1 = 0.3$ms, and a maximum Q-factor $Q_i = 7.1 \times 10^6$. These values are slightly higher than the best Nb SCPW resonators as of current ($Q_i = 3.2 \times 10^6$) [30]. Another study by Barends et al. [102] measured almost identical Q-factors in Nb and Ta resonators on Si substrates, suggesting that sapphire is a more suitable substrate for use with Ta films. These results will surely prompt enquiry into Ta on sapphire as a material platform for SC circuits. Other successful superconducting materials and their current best Q-factors can be found in Table 2.1. In our study, Al was chosen as the superconducting material due to the ease of fabrication and instant availability for deposition at UQ, which is important due to the one year time-limit of this project.

Substrate materials

Due to the wide range of semiconducting or insulating crystalline materials available, the range of suitable choices of substrates for SCPW resonators is broad. Substrates suitable for high-Q SCPW resonators should have low dielectric losses and allow for non-destructive surface preparation resulting in a low-roughness, atomically perfect surface. A smooth substrate surface will allow for uniform grain nucleation when growing the SC film, resulting in a more uniform distribution of polycrystalline grains in the film [22]. Additionally, an atomically perfect, defect free substrate surface will host fewer TLS that could otherwise be present in defects or dangling bonds [32, 97]. Lattice-matching, which we will discuss further in the next section, also impacts the quality of film growth and SM-interface defect-density [7, 67]. For this reason the best substrate choice depends on the choice of SC material. For example, in Table 2.1 it can be seen that sapphire is to date the most successful substrate for Al SC films. Si is the most common choice of substrate due to its accessibility, low dielectric losses, and compatibility with classical integrated circuits [86]. Furthermore, surface treatments of Si are well understood both experimentally and theoretically, allowing researchers to follow trusted recipes for atomically accurate surface termination [55, 56]. It has been shown that passivation treatments of Si surfaces are effective in improving the quality of Si-based resonators [40, 78, 106, 107]. Sapphire also has well-known wet-chemical surface treatments [60]. A study by Megrant et al. [53] has shown the importance of a well-treated sapphire substrate, with rougher or adsorbate-rich surfaces contributing highly to resonator losses. Surface treatments for other non-standard substrates, such as LAO [108], have been reported, however the effectiveness of these treatments in the context of high-Q SCPW resonators is yet to be explored. Table 2.1 shows the highest-Q resonators measured to date for each substrate-film material platform.

Lattice matching

Well matched lattice constants and crystal structure between the substrate and film material facilitate uniform heteroepitaxial film growth [7, 33]. With a small lattice mismatch between

the substrate and film, the SM interface will be more coherent, with fewer lattice dislocations and/or less strain. This is shown in figure 2.6. Since TLS can arise from dangling bonds at lattice dislocations, and from defects produced in strained film growth, a highly lattice-matched system should have few TLS associated direction with film nucleation and growth. This reduction of TLS should translate to a higher Q resonator.

Al has a lattice constant a of $a_{\mathrm{Al}} = 0.405\mathrm{nm}$ [74]. The substrate materials used in this study, LAO and MAO, have lattice constants of $a_{\mathrm{LAO}} = 0.379\mathrm{nm}$ [68, 109] and $a_{\mathrm{MAO}} = 0.808\mathrm{nm}$ [71, 72]. MAO has a negligible lattice mismatch with Al, whilst LAO has a mismatch around 6%.

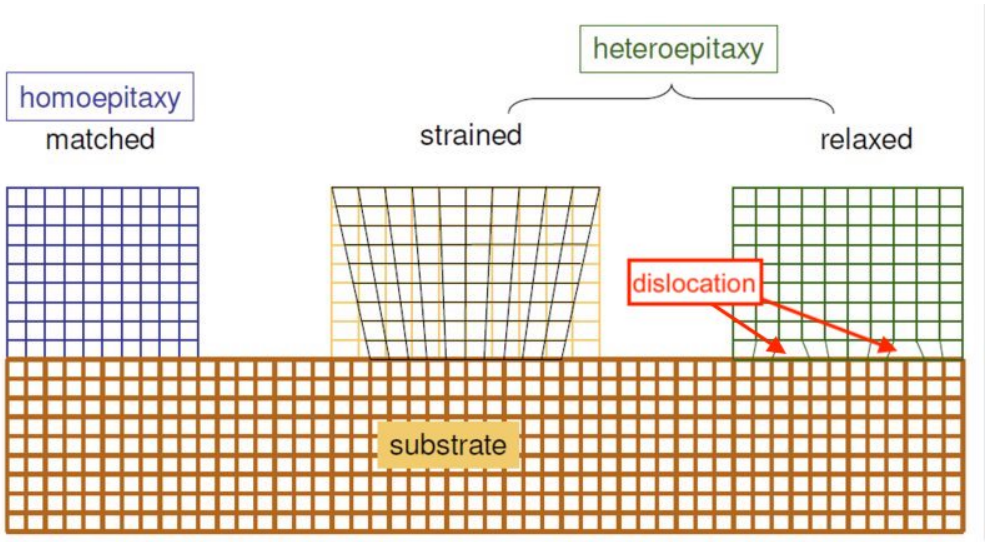


FIGURE 2.6: Visualisation of homo- and heteroepitaxial film growth in a lattice-mismatched system. Homoepitaxy can occur with lattice-matched materials, and either strained or relaxed heteroepitaxy can occur in lattice-mismatched systems, as is the case in the SCPW substrate-film systems. Systems with larger lattice mismatch will have either a higher number of dislocations in relaxed heteroepitaxial growth, or larger interfacial strain in strained heteroepitaxial growth. Both outcomes will negatively impact the quality and uniformity of film nucleation and growth [7]. Figure taken from [8], with added label for dislocations in relaxed heteroepitaxy.

2.2.2 Fabrication protocols

Fabrication of a SCPW resonator generally consists of the following steps: 1) substrate surface treatment; 2) thin film deposition; 3) spin coat and soft-bake of photoresist; 4) lithography of resonator design; 5) liftoff or etching of photoresist; 6) removal of photoresist and final clean; 7) contamination-free storage [22, 86]. Losses at device interfaces have been shown to contribute significantly to the overall loss of a SCPW resonator [43], there has therefore been increased focus on cleaning and deposition techniques in order to minimise and understand these losses [111]. In particular, the SM interface may be the largest contributor to TLS losses [30, 54]. Therefore pre-deposition substrate cleaning procedures are especially important. It has also been shown that defects induced during the lithography stage of

SC	Substrate	Q_i (millions)	Year	Reference
Nb	Si	3.2	2020	Altoe et al. [30]
Ta	Al_2O_3	7.1	2020	Place et al. [50]
TiN	Si	2.2	2018	Calusine et al. [54]
TiN	Si	1.5	2019	Woods et al. [44]
NbN	Y_2SiO_5	0.4	2019	Dold et al. [110]
Al	GaAs	0.4	2020	Scigliuzzo et al. [93]
Al	Al_2O_3	5.3	2016	Richardson et al. [45]
Al	Si	1.0	2017	Dunsworth et al. [52]

Table 2.1: The current highest Q resonators for each material combination. Note that resonators are built over a range of scales, and with different geometries, each of which will also impact the measured Q_i [21]. Furthermore, experimental design varies; the results should not be directly compared. All measurements listed here were taken in the 'quantum' regime: low-temperature ($\sim$ 20mK) and $\langle n_{ph} \rangle = 1$. A larger summary of recent successes in high-Q SCPW resonator fabrication, including materials and fabrication method, can be found in McRae et al. [22].

fabrication can result in reduced Qs [45, 96, 107]. Whilst there is not a preferred lithography method, liftoff procedures have been optimised to minimise TLS losses [52, 111]. Leftover photoresist from etching procedures could contribute to TLS losses. Removal of photoresist in etch-based methods could be further optimised, for example by super-critical carbon dioxide (CO_2) cleaning [112], which we hope to test in future research. A good storage method should not introduce any contamination to the sample between fabrication and operational testing.

2.2.3 Chip design and geometry

The geometry of a TL-coupled SCPW resonator determines TL and resonator impedance (Z_0 and Z_r respectively), coupling strength and type (capacitive or inductive) between the TL and resonators and resonance frequencies [15]. The impedances are primarily impacted by the S/W ratio (gap size (W) to width (S) size, as shown in figure 1.1). The coupling strength is determined by the coupling length, as shown in figure 2.1a), and the distance from transmission line to resonator, which is equal to 24µm in figure 2.1b). The fundamental frequency and higher mode frequencies of each resonator are determined by the total resonator length according to equation 2.10 [15, 87]. In practice, the frequency will be slightly shifted due to the TL coupling; a larger coupling strength will result in a larger frequency shift. The frequency shift will be on the order of MHz [15], so resonators can be designed at a certain frequency to acceptable accuracy using equation 2.10. To tune impedances, coupling strengths and resonant frequencies, the permittivity of the substrate must be known. In this study, we do not test resonator Q as a function of geometry. Instead, we keep the geometry constant (with minor adjustments to account for substrate permittivity) and vary materials and fabrication protocols.

A well-designed SCPW resonator should seek to minimise coupling to parasitic TLS and

to minimise unwanted coupling between circuit elements [21]. For example, if parallel lines of a resonator meander are too close there may be weak coupling between them, affecting both the resonant frequency f_0 and Q of the resonator. This could also occur if too many resonators are coupled to a single TL for the space available on the chip. Coupling to TLS can be avoided to some extent by maximising the electric field mode volume in the resonator which in turn reduces the electric field density in TLS-hosting volumes such as surface oxides. Therefore, the participation of TLS towards resonator properties is reduced, resulting in an improved Q [21, 46, 113]. However, a bigger circuit is not necessarily better; a SCPW resonator circuit that is too large will not be highly scalable.

3 Characterisation methods

In this study, we use a combination of three characterisation techniques to measure changes to the topographical and chemical structure of surfaces at multiple points throughout the fabrication process. Atomic force microscopy (AFM) in tapping mode is used to measure properties such as surface roughness, Al film grain size and to monitor changes in surface structure. We use X-ray photoelectron spectroscopy (XPS) to measure changes to the atomic concentrations and chemical state of atoms on surfaces throughout fabrication. X-ray reflectometry (XRR) is used to measure the thickness of our Al film. In this section we discuss the operating principles, methods of analysis and relevant theoretical background for each of the surface characterisation techniques.

3.1 Tapping mode atomic force microscopy (AFM)

Atomic force microscopy (AFM) is a tool to used to investigate the 3D surface structure of both insulating and conducting samples. The first AFM was developed by Binnig, Quate and Gerber in 1986, only five years after they invented the scanning tunnelling microscope (STM) [114]. Their AFM had a lateral resolution of 30Å and a vertical resolution of 1Å [114]. The resolution was then further improved by Meyer et al. in 1988 by implementing an optical (as opposed to electrical) detection circuit [115]. The development of AFM was born out of the need for an STM equivalent that was effective for insulating samples [114]. Since STM relies on the tunnelling current between the probe tip and the sample, the technique is not effective on insulators [10, 114, 116]. For the first time, AFM made it possible to investigate insulating samples below the diffraction-limit of optical microscopy [117]. In particular, this made it possible to study the structure of many biological samples at atomic resolution.

In this study, we exclusively use AFM in non-contact tapping mode, which is one of many possible operating modes [116]. Here, we discuss the basic operating principles of tapping mode AFM, the corresponding theory, and the common methods of data analysis.

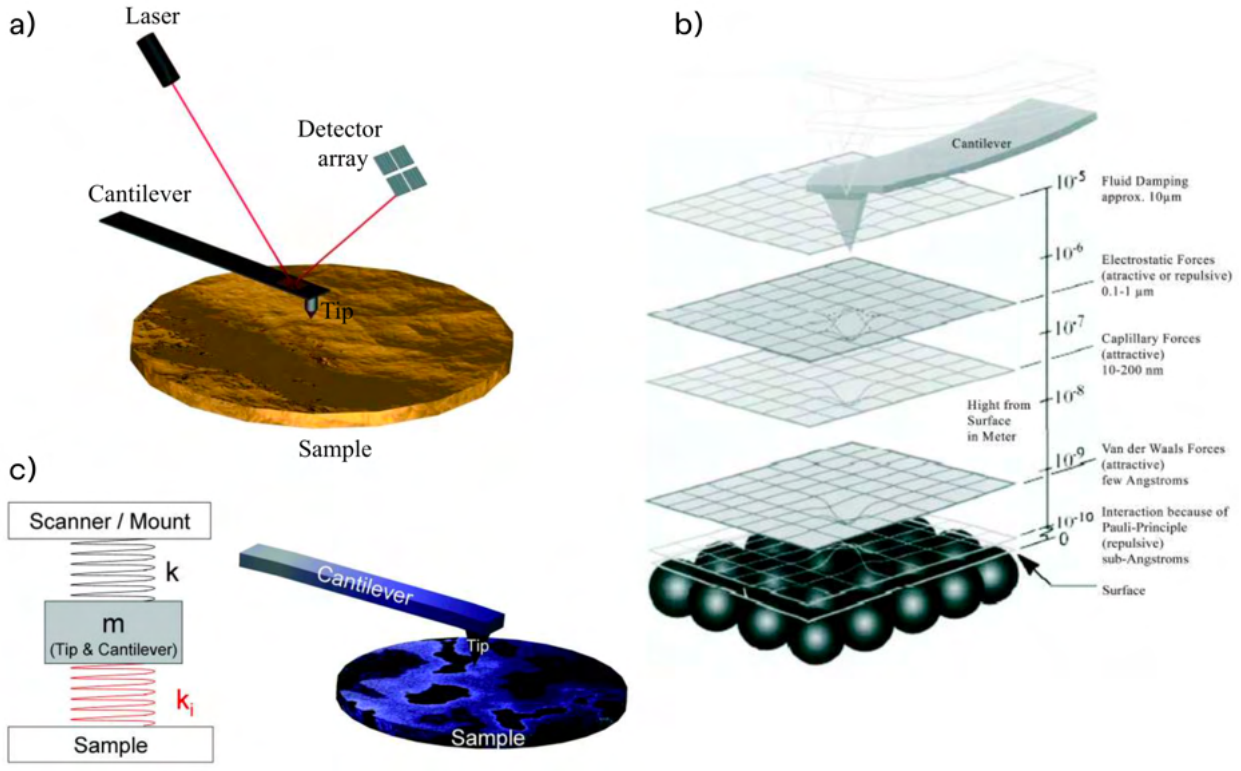


FIGURE 3.1: **a)** Graphic representation of the working principle of atomic force microscopy (AFM). We see a tip attached to a cantilever, which is raster scanned over a surface by a digitally controlled xyz scan stage. The tip deflections are measured by an optical detection setup, in which a laser is reflected off the cantilever into a photo diode detector array. **b)** Force regions in proximity to a surface. As the tip moves from 10µm to the surface, it will pass through regions where attractive forces dominate, and regions where repulsive forces dominate. **c)** A simple spring model originally used by Giessibl [9] to calculate the cantilever frequency shift as a function of the surface force. The tip-surface interaction is modelled as a spring with spring constant k_i. The cantilever is taken to have a spring constant k and mass m. Images modified from Herden [10].

3.1.1 Basic operating principles

In AFM, a sharp tip is attached to the end of a cantilever which is scanned over the surface under investigation. The cantilever is driven at its free-space (meaning free of surface interactions) resonance frequency f_0 by a piezoelectric at a set amplitude A typically from 10 - 100nm. Forces acting between the sample surface and the tip cause the oscillation frequency and amplitude to shift from the free-space values. By measuring the deflection of the tip from its free-space oscillations, the surface forces can be mapped in the xyz plane [116]. Most commonly, these deflections are measured by reflecting a laser off the back of the cantilever, and detecting it with a photo diode array, as shown graphically in figure 3.1a [10].

In STM, there is a unique dependence between tip-sample distance and the tunnelling current, making it relatively straightforward to measure surface topography by detecting the tunnelling current [116]. In AFM, the imaging process is not as straightforward. This is due to the fact that the AFM tip feels a range of forces over its range of motion, as shown in

figure 3.1b. The functional relationship between the system's measurable parameters (such as amplitude or frequency) and the surface force is more complex than in the case of STM [118]. At different surface-tip distances, the dominating force changes. In some regimes, the dominating force will be attractive, whilst in other regimes the tip-surface force is repulsive. In general, the different imaging modes of AFM make use of a particular force region. For example, in contact mode the tip is dragged across the surface, being repelled due to Pauli repulsion force

An AFM tip typically has a radius of curvature from 2 - 20nm. The lateral resolution of the image is limited by the tip sharpness as a blunter tip will feel force contributions from a larger set of surface atoms. It is not uncommon to have a tip snap, or a contaminant attach itself to the tip when imaging. In either case, such an event can be tracked by noticing a loss in imaging resolution. In general, tip contamination could be removed by blow-drying the tip with nitrogen, or by chemical etching. The oscillation amplitude of the AFM tip is determined by the drive amplitude and the cantilever spring constant, which typically lie in the range of 0.1 - 10N/m. For contact mode imaging, very low spring constants are chosen to minimise surface damage. In tapping modes, we use higher spring constants to reduce the oscillation amplitude, improving the vertical resolution.

In this study, we use non-contact tapping mode AFM, which is a non-destructive, dynamic imaging mode. In tapping mode, the cantilever is oscillated at a small amplitude ($A \sim 1$nm) at its free-space resonance f_0. Both frequency and amplitude modulation to the free-space oscillation, as well as the phase between the piezoelectric oscillations and the tip is measured by the optical detection circuit. Tapping mode modulations occur primarily due to attractive Van der Waals forces and short-range chemical forces. Frequency and amplitude feedback loops give information on the topographical surface structure, whilst the phase loop reacts to mechanical properties of the surface [10].

3.1.2 Theoretical principles

A simple spring model of an AFM tip reacting with a surface is visualised in figure 3.1c, where the interaction between the tip and surface is modelled as a spring with spring constant k_i. We take the cantilever to have a spring constant k, and a mass of m. When the tip is not reacting with the sample (i.e. beyond the range of surface interactions), the resonant frequency f_0 of the cantilever is given as

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{k}{m}}. \tag{3.1}$$

We now add in the effect of the surface interactions using the simple spring model, where the frequency is shifted according to

$$f = \frac{1}{2\pi}\sqrt{\frac{k + k_i(z)}{m}}. \tag{3.2}$$

This equation assumes that the effective spring constant k_i is constant over the z-range of oscillations. In general, this is untrue. To resolve this, Giessibl used perturbation theory to

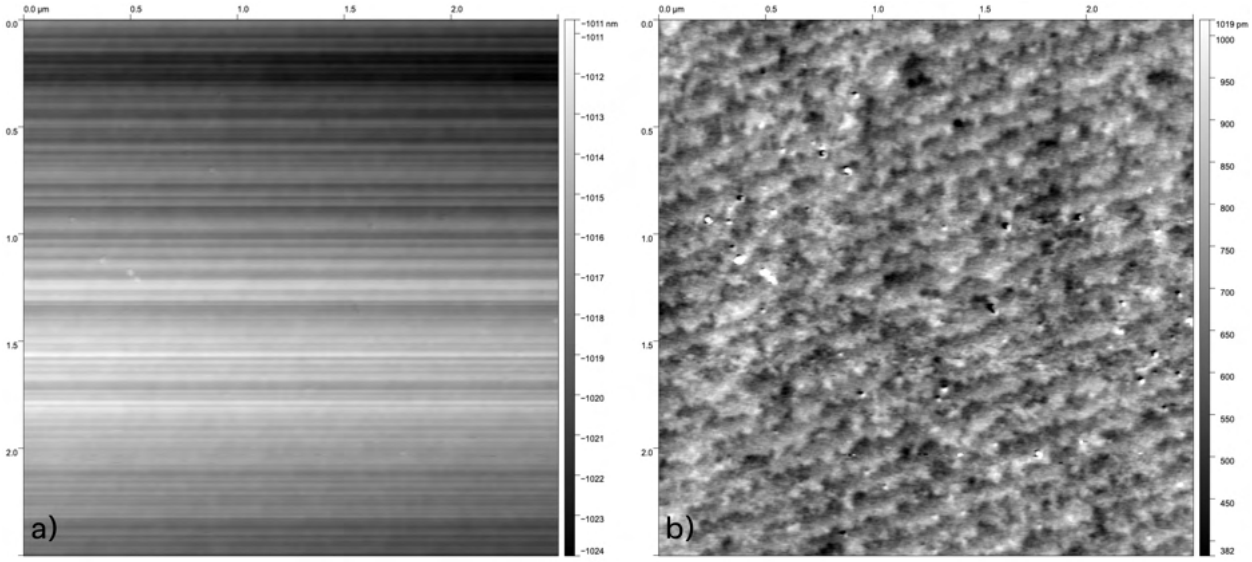


FIGURE 3.2: AFM image of an as-recieved LAO surface. Image **a)** shows the unprocessed (raw) AFM data, whilst **b)** shows the image after basic process steps which consisted of line matching, background flattening, and horizontal scar correction. The image was processed with inbuilt features of `Gwyddion`. The AFM image was taken at ANFF-Q on an Asylum Instruments Cypher AFM using a TAP300GD-G tip ($<$ 10nm nominal tip radius, $k = 40$N/m) in tapping mode.

calculate an average spring constant $\overline{k_i(z)}$ that would result in an accurate frequency shift $\Delta f = f - f_0$ [9]. Assuming that $\overline{k_i(z)} \ll k$, the frequency shift can be approximated as

$$\Delta f \approx \frac{\overline{k_i(z)}}{2k}. \tag{3.3}$$

This condition is generally satisfied in reality by choosing a cantilever with a large spring constant ($k \geq 3\mathrm{N\,m^{-1}}$). Using the Hamilton-Jacobi perturbative approach, Giessibl found

$$\overline{k_i} = \frac{2}{\pi}\int_{-1}^{1} k_i(z - Au)\sqrt{1-u^2}du, \tag{3.4}$$

where u is the parametrisation parameter of the oscillation. Equation 3.4 gives the force (k_i) as a function of the oscillation, however in reality we measure the oscillation and want to derive the forces. This requires inverting equation 3.4. This was achieved by Sader and Jarvis, who found a formula to describe the forces in terms of the measured frequency shift to 5% accuracy [119].

3.1.3 AFM image analysis

Information on the topographical surface structure, surface roughness, and chemical changes on the surface can all be measured by tapping mode AFM. To extract meaningful information from an AFM image, careful analysis must be performed. It is quite easy to process an AFM image in such a way that the extracted value, for example roughness, is not physically

accurate. This could be due to the image being *flattened* during processing, which in effect decreases the roughness of the image. For an in-depth discussion of AFM image analysis, see the paper by Nečas et. al [120]. Here we discuss the methods used for AFM image analysis, which was done using software programs `ImageJ` and `Gwyddion`, both of which are cross-platform freeware. Here, we discuss analysis in the context of `Gwyddion`, however equivalent processes apply to `ImageJ`. In this study, we follow a set process of image editing for consistency across images and samples.

An example of a raw (unprocessed) and processed AFM image is shown in figure 3.2. The tip's scan direction is clear in the raw image, where horizontal scan lines can be seen. Most AFM software scales the data along each scan line by the line's average value. This is why the raw image appears smooth in the x-direction, but not in the z-direction. This can be resolved by using Gwyddion's `align rows` feature, which presents multiple algorithms for line-matching. We use the *matching* method on Gwyddion for all image processing. This method of line matching was found to preserve the roughness information. Once the line-matching is complete, it may be desirable to correct a background tilt in the sample. This can be done through various flattening techniques, such as the removal of a background plane, or by polynomial background subtraction. In the case of background plane removal, roughness data will be preserved, however it will be inaccurate after a polynomial background subtraction. In the case of figure 3.2, a simple background plane correction was performed. Horizontal 'scars', a common artefact of AFM imaging, can be removed by the `correct horizontal scars` feature on Gwyddion. This is mostly an aesthetic processing step, however it can help improve the accuracy of roughness measurements. A 'scar' with a large height value could drastically increase the measured roughness of the surface. Once the image is processed as intended, the surface roughness can be measured with the `statistical quantities` feature in Gwyddion, which gives RMS and mean roughness, as well as a number of other useful statistics.

Figure 3.3 shows height and phase data from the same AFM image of Al film grains on an LAO substrate. Note that these two data channels are recorded simultaneously in the same physical scan. As mentioned earlier, differences in phase correspond to viscoelastic properties of the surface. Certain surfaces can be *stickier*, causing more delay between the drive and tip oscillations (corresponding to a larger phase value). Generally, the stickiness of a surface is a function of its chemical makeup. In relation to figure 3.3, the phase image tells us the chemical composition at the grain boundaries is not the same as the bulk properties. As we will see later, this phase information can be used in conjunction with chemical surface data obtained by XPS to make strong conclusions about the chemical structure of surfaces. In this study, we also used phase images to measure the size and distribution of grains, as the contrast between grains is more pronounced in a phase image. This was done using the watershed method of grain detection, implemented in Gwyddion.

3.2 X-ray photoelectron spectroscopy (XPS)

In X-ray photoelectron spectroscopy (XPS), high energy X-rays move through vacuum to bombard the surface of the sample under investigation. The X-rays have enough energy to

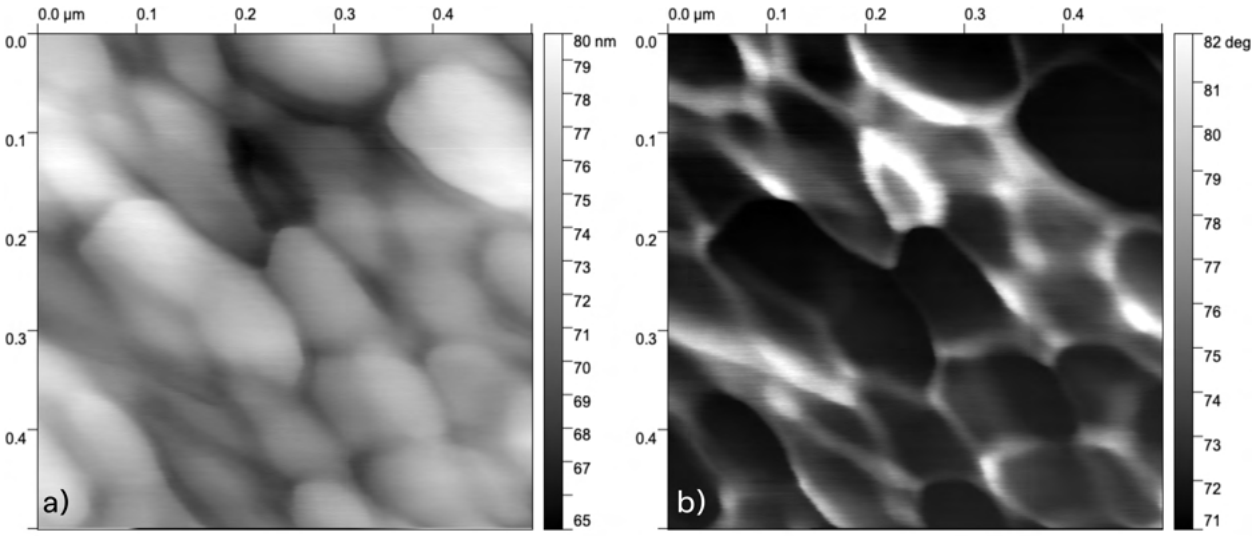


FIGURE 3.3: AFM image of Al film grains grown by E-beam evaporation on an LAO substrate. Image **a)** shows the AFM height data, whilst **b)** shows the phase data. Changes in the phase values correspond to differences in the chemical structure on the surface. Here, the phase image shows that the grain boundaries have a slightly different chemical structure (perhaps, higher oxide density) than the bulk of the grains. The image was processed with the inbuilt background plane subtraction feature of `Gwyddion`. The AFM image was taken at ANFF-Q on an Asylum Instruments Cypher AFM using a TAP300GD-G tip ($<$ 10nm nominal tip radius, $k = 40$N/m) in tapping mode.

eject even the most tightly bound electrons from their atomic orbitals, inducing a photocurrent. These ejected electrons are then guided towards a detector with external electric fields, where their kinetic energies are measured. By accounting for the incident radiation's energy, and the work function of the surface from which they were ejected, the binding energy of the electrons can be calculated. As each element has a unique set of binding energies, an 'energetic fingerprint', the density of measured electron energies gives information about the atomic content of the surface [121]. This is possible due to the fact that a spectrum obtained from a mixture of elements is equal to the sum of their peaks [121].

XPS was developed by Seigbahn in the mid 1960s, for which he was awarded the Nobel Prize in 1981. By that time, XPS was being relied on in laboratories across the world. Here, we discuss common X-ray sources for XPS, the basic operating principles, and methods of data analysis. In this study, all XPS measurements were done on a Kratos Axis Ultra XPS located in the Centre for Microscopy and Microanalysis (CMM) at UQ.

3.2.1 Monochromatic X-ray sources

X-rays have a shorter wavelength than visible light, and are therefore more energetic. X-ray wavelengths are in the range of 0.02 - 100Å, which is within the range of typical crystal lattice constants. This makes them a very attractive probe for examining the properties of crystals. There are many X-ray diffraction techniques (including XRR, which we will see in section 3.3) which can extract bulk crystal properties of a sample, however XPS is only interested in the surface of a sample. In this case, it is the high energy and relatively

straightforward generation of X-rays that make them the probe of choice for this technique.

The Kratos Axis Ultra XPS used in this study has a monochromatic Al Kα (1486.6eV) X-ray source [122]. Al Kα_1 radiation has a penetration depth on the order of 1 - 10µm. X-rays are generated in a vacuum X-ray tube which consists of a tungsten filament (cathode) and a metal target (anode). Electrons are ejected from the tungsten filament by thermionic emission, which is induced by running a current through the filament. A large voltage difference around 30kV is applied between the cathode and anode, accelerating the electrons towards the anode. When the accelerated electrons hit the anode, the inner shell electrons are dislodged. This leaves a vacancy in the inner shell, which is quickly filled by an electron from a higher orbital. As this electron falls into the inner shell, an X-ray photon is emitted [123]. The notation Kα means that an electron from a 2p orbital filled the 1s vacancy left by the ejected electron.

To maximise the resolution of XPS measurements, which is typically on the order of 1eV, the linewidth of the X-ray source should be minimized [123]. This sets tighter bounds on the binding energy of the orbital from which the detected electrons were ejected (as we will see in equation 3.5). Typically, lighter elements are used as the linewidth of the generated X-ray radiation is dependent on the atomic number of the element from which it was generated [121]. The X-ray source can be further improved by using a monochromator filter the radiation. Typically, monochromators use a single crystal to constructively diffract a particular wavelength, whilst other wavelengths destructively interfere. The wavelength to isolate can be chosen by changing the angle of incidence onto the monochromator lens, which in turn changes the distance between the crystal planes that reflect the signal.

3.2.2 Operating principles

Surface characterisation by XPS is done by irradiating the sample surface with X-rays of a known energy, and measuring the energy spectrum of the ejected electrons [121]. X-rays can penetrate relatively far into a solid due to their high energies. However, when an electron is ejected from its orbital (as is the case in XPS) in the bulk of a solid, it will not make it out to the surface without losing most of its energy due to collisions; the mean free path of electrons in a solid is very small [121]. This makes XPS a surface technique that will only obtain electron energy spectra from the first few atomic layers of a sample; it is not a bulk characterisation technique. The kinetic energies of the ejected electrons are measured, and can be related to the binding energy of the orbital from which they were ejected by

$$KE = h\nu - BE - \phi, \tag{3.5}$$

where KE is the kinetic energy of the electron measured by the detector, ϕ is the work function of the surface, $h\nu$ is the energy of the incident X-rays, and BE is the binding energy of the orbital from which the electron was ejected [121]. As mentioned in the previous section, tighter bounds on the incident X-ray energy $h\nu$ allows for tighter bounds on the binding energy BE.

XPS takes place under vacuum as it is important that the majority of ejected electrons are able to travel from the sample to the detector without a collision. If too many electrons have collisions on the way to the detector (as would be the case in ambient conditions),

the measured energy spectrum will no longer be representative of the surface chemistry. Electrons that collide with matter in space, or collide with atoms on their way out of the bulk of the material, make up the background signal that is seen in all XPS measurements. In the following section, we discuss how this is accounted for during data analysis.

In this study, we characterise both the LAO and MAO substrates at multiple points throughout their surface treatments. Both MAO and LAO are insulators, so as the surface is gradually ionised by the incident X-rays during measurement the net charge of the sample goes positive. This will result in XPS peaks' energies being shifted to higher binding energies as the measurement continues. This can be rectified by applying a controlled flux of electrons to the sample in order to keep the net charge constant at zero over the course of measurement. The magnitude of electron flux required for neutralisation can be calibrated by taking repeated measurements of a particular peak (normally the C 1s peak) and tracking the peak's shift. Once the peak remains stationary at a particular value, the neutralisation magnitude is correct and measurement can begin [121].

3.2.3 Data analysis

There are two primary modes of data acquisition in XPS; survey scans and high resolution scans. An example of each is shown in figure 3.4. A survey scan is done over a large range of binding energies, typically 0 - 1100eV, and gives information on the surface's atomic concentrations. High resolution scans focus on a peak corresponding to a particular orbital, and give information on the chemical state of this element on the surface.

Analysis of XPS data relies on comparison of collected spectra with standard spectra, such as those presented in the XPS Handbook [121]. The standard spectra give the binding energy, and peak shapes of the characteristic XPS peak for each element. For example, if we find that our O 1s has an additional component compared to the standard O 1s peaks, this would mean that we have a non-zero concentration of oxygen in a different chemical state (for example, bonded with hydrogen). The C 1s peak at 284.8eV is typically used to calibrate the measurement, as carbon is present on almost all laboratory sample (irregardless of the bulk material), and has a well defined peak centre. To calibrate the data, the C 1s peak should be located on a survey scan, and the entire spectrum should be shifted such that the C 1s peak is centred at 284.8eV [121].

In this study, we use the software `CasaXPS` to visualise and analyse our XPS data. `CasaXPS` has an extensive inbuilt library of standard elemental data including (but not limited to) binding energies, masses and relative sensitivity factors (RSFs), which relate the measured area of a certain peak to the atomic concentration of the corresponding atom. The software also has multiple inbuilt Gaussian and Lorentzian fitting and background approximation algorithms. These functions are used to estimate the (background subtracted) area of a certain peak, atomic concentrations and chemical components in a high-resolution peak. Figure 3.4a shows an example survey scan with the measured binding energies, peak areas and atomic concentrations. The corresponding peak parameters, as displayed in CasaXPS, are shown in figure 3.4b. In figure 3.4c, an example spectrum of the O 1s peak at 531eV, and the background approximation, is shown. To determine the area of the peak, CasaXPS fits Gaussian functions to the peak.

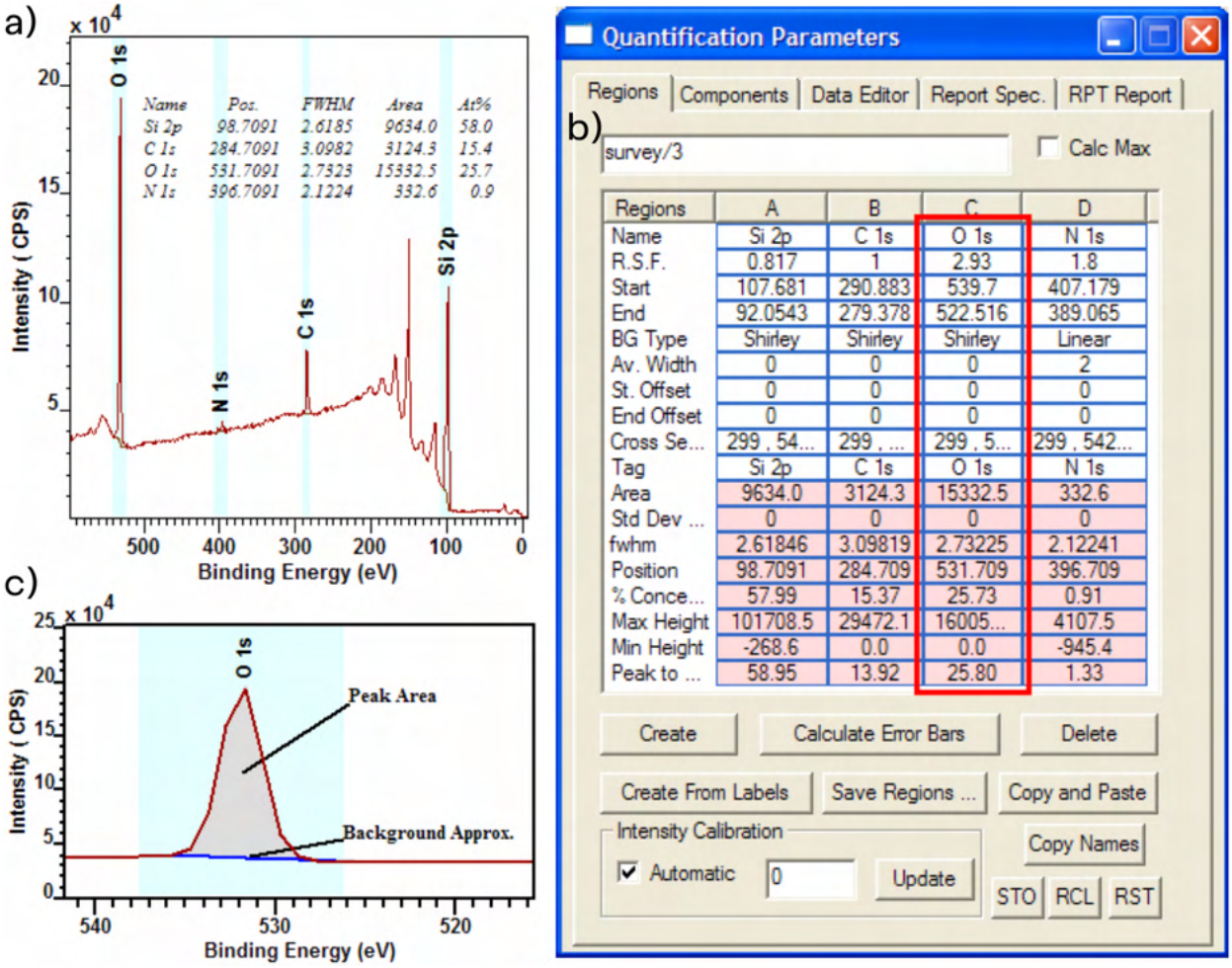


FIGURE 3.4: Here we see XPS data visualised in CasaXPS. Image **a)** shows a high resolution scan with the corresponding peak names, binding energies (*Pos.*), full-width half-maximum (*FWHM*), peak area and atomic concentration given as a percentage (*At%*). In panel **b)**, we see the region parameters corresponding to the survey scan in a). The R.S.F. (relative sensitivity factor) scale the peak areas to give physically accurate atomic concentrations. In this survey scan, the Shirley algorithm was chosen as the method of background subtraction. Panel **c)** shows a high resolution scan of the O 1s peak, with the background approximation visualised. The area of the peak is shaded in light red. Figure taken from the CasaXPS handbook [11].

3.3 X-ray reflectometry (XRR)

The X-ray reflectometry (XRR) measurement technique is used to analyse intensity curves of reflected grazing incident X-rays. The sample is irradiated with monochromatic X-rays at an incidence angle of θ, and the reflected intensity (again at an angle θ) is measured by a detector. The method gives information on the thickness, density and interface roughness of thin-film structures. XRR is a robust characterisation technique, allowing for examination of crystalline, polycrystalline (as in the case of our Al films), and amorphous materials [12].

The technique also has the advantage of being non-destructive. Here we discuss the basic operating principles and methods of analysis. We used a Rigaku Smartlab XRD system, located in CMM at UQ, to perform the XRR measurements. For all measurements, monochromatic Cu Kα X-rays were used, which have an energy of 8.05keV and a corresponding wavelength of $\lambda = 1.54$angstrom.

3.3.1 Operating principles

When electromagnetic radiation is incident on a surface, some proportion of the radiation is reflected, and some proportion is refracted into the material. At incidence angle less than the critical angle θ_c of the material under investigation, total reflection occurs. Beyond the critical angle, the reflected intensity decreases proportional to θ^4 [12]. The critical angle of a material is related to its density. In XRR, the thin film layer is differentiated from the substrate by a difference in electron density. For this reason, XRR is not suitable for a film that has an electron density very close to that of its substrate. Furthermore, this technique will not work for thick films, as the X-rays will not be able to penetrate far enough to reflect off the film-substrate interface. The exact penetration depth is dependent on the film material and incident X-ray energy.

For our use case, we consider the workings of XRR on a two layered structure with a dielectric substrate and a $\sim$ 100nm metal film. Some of the scattered X-rays come from reflections off the film surface, whilst others come from reflection off the substrate surface at the substrate-film interface (referred to as the MS interface in the quantum hardware realm). These two reflected rays will interfere either constructively or destructively depending on the film thickness and incidence angle (since the incident wavelength is kept constant). Therefore, as the incident angle is changed, we see oscillations in the reflected intensity due to the changing interference between the two reflected waves. This phenomena was first observed by Kiessig in 1931, earning the oscillations the title of Kiessig fringes [124]. The fringes are shown in figure 3.5, where we see that the film thickness d can be estimated from the period $\Delta\theta$ of oscillation. The amplitude of the Kiessig fringes are dependent on the electron density difference between the film and substrate, and the high angle decay of Kiessig fringes is dependent on the surface and surface or interface roughness. The decay of the reflected intensity depends on the film's surface roughness. Whilst it is possible to calculate surface roughnesses from XRR, we do not require this information as the surface roughnesses are directly measured by AFM in our case.

3.3.2 Analysis with Motofit

In this study, we analyse XRR data with `Motofit`, which is cross-platform freeware [20]. `Motofit` uses the Ables [125] formulation to calculate the specular reflectivity $R = I_{ref}/I_{in}$, which is defined as the ratio of reflected intensity against incident intensity. The algorithm uses a slab structure, where layers of thickness d_n, scattering length density ρ_n and surface roughness $\sigma_{n,n+1}$ are stacked on top of each other. The reflectivity spectrum is then simulated by calculating the Fresnel reflection coefficient at each interface, and each layer's parameters are adjusted until a best fit with the experimental data is found. Interfacial roughness

is accounted for by adjusting the Fresnel reflection coefficient describing reflections from the rough interface according to the method described by Nevot and Croce [126]. The fit parameters are optimised with a genetic algorithm, which has the advantage of allowing for initial parameter guesses (such as film thickness d) to be far from the correct solution. This means that a suitable fit for XRR data can be found without in-depth prior knowledge of the sample features [127].

In our case, we wish to extract the film thickness d from our XRR data, which we know (from thickness monitoring during E-beam evaporation) is around 100nm thick. This corresponds to the period of Kiessig fringes in a XRR data plot such as that in figure 3.5. This means that we do not need our fit to account perfectly for surface roughnesses and the density contrast between the film and substrate (i.e. the amplitude and decay of Kiessig fringes). In the case of Al on MAO, the density contrast is quite small; $\rho_{\mathrm{Al}} = 2.7\mathrm{g\,cm^{-3}}, \rho_{\mathrm{MAO}} = 3.5\mathrm{g\,cm^{-3}}$. This makes the fitting of interfacial roughness and density contrast difficult. In the case of LAO, the density contrast is much larger, $\rho_{\mathrm{LAO}} = 6.4\mathrm{g\,cm^{-3}}$.

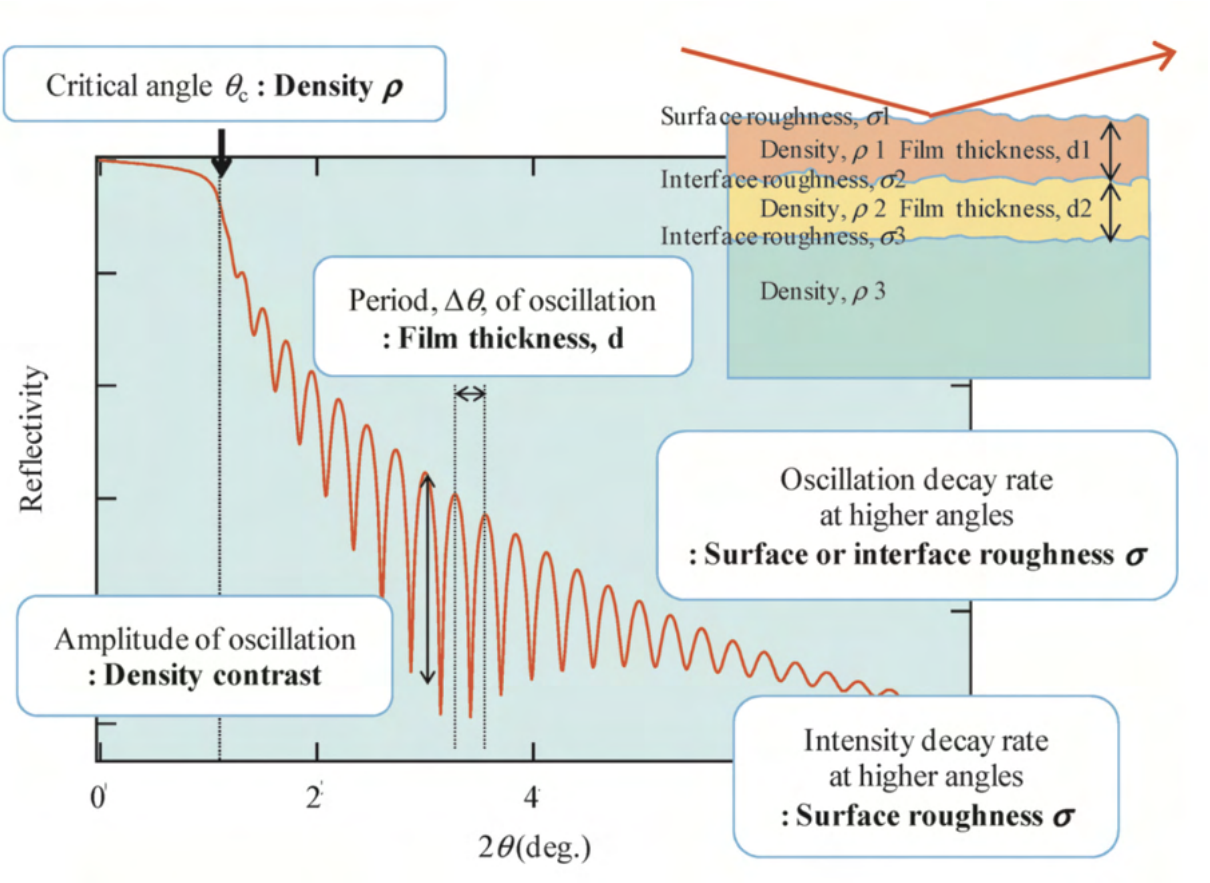


Figure 3.5: Example XRR data from a three-layer structure consisting of a substrate and two thin film layers. The plot shows the reflected intensity as a function of the incidence angle θ, which is equal to the detector angle (hence the x-axis label 2θ). A number of values can be extracted from an XRR measurement including film thickness d and density ρ, the film surface roughness σ_1, the interface roughnesses σ_2 and σ_3, and the density contrast between layers. Figure taken from Yasaka [12].

4
Fabrication methods

Material losses are a quality-limiting loss channel for SCPW resonators [1, 2, 21, 48, 58]. By designing a contamination-free fabrication protocol in which amorphous surface oxides and defects in the superconducting film are minimised, higher quality resonators can be produced [22]. Furthermore, sub-micron accuracy must be achieved during the lithography stage of fabrication to ensure the chip design is patterned with the intended geometry. A mis-printed device could suffer from issues due to impedance matching, feedline to resonator coupling, short-circuiting and many others [87]. In this section we discuss the methods used to fabricate our SCPW resonators as well as considerations for future fabrications.

The devices fabricated in this study are two layer structures consisting of a 100 nm thick superconducting aluminium film deposited on top of a dielectric substrate. We fabricated devices on LAO and MAO substrates, with thicknesses of 500µm and 1000µm respectively. The chip's design is then patterned directly onto the superconducting layer. After this, the chips are diced into separate circuits that can be wire-bonded onto an external printed circuit board (PCB). In general, a device of this nature is fabricated as follows.

1. Substrate preparation (annealing, wet chemical cleaning)
2. Film deposition
3. Lithography
4. Dicing
5. Wire-bonding

Both the LAO(100) and MAO(100) substrates were purchased directly from MTI Corporation. The final devices were fabricated on 25.4 x 25.4 x 0.5mm thickness, 2 side epi-polished LAO(100) wafers, and 20 x 20 x 1.0mm thickness, 1 side epi-polished MAO(100) wafers. We also obtained a number of smaller substrates to test the fabrication process on. A summary of the fabrication recipe for both the LAO and MAO devices is shown in table 4.1.

	MAO	**LAO**
Pre-anneal clean	5 minute sequential sonication in acetone, IPA and DI water, blow-dry with nitrogen gas	Same as MAO
Anneal	1100°C for 5 hours in O_2 at a flow rate of $0.5\,\mathrm{l\,min^{-1}}$	1200°C for 3 hours in O_2 at a flow rate of $0.5\,\mathrm{l\,min^{-1}}$
Post-anneal treatment	5 minute sonication in DI water, blow-dry with nitrogen gas	120 minute sonication in DI water, blow-dry with nitrogen gas
Deposition	100nm Al film deposited via E-beam evaporation at 0.5nm/s	Same as MAO
Spin coating	AZ1512-HS photoresist, spin coated at 5800RPM for 60s (1.3 ± 0.2µm thickness)	Same as MAO
Post-spin softbake	60 seconds at 110°C on metal hot-plate	Same as MAO
Exposure	Direct-write optical lithography, with 45mW laser at 25% intensity	Same as MAO
Development	45 seconds in AZ726 MIF developer	Same as MAO
Etching	35 seconds in Al etchant	same as MAO
Dicing	Microkerf Minitron 2.187-8-45H diamond blade with 10KRPM spindle speed, 0.1mm/s exit and entry speed, and 0.5mm/s cut speed	Same as MAO

TABLE 4.1: Fabrication recipe and parameters for CPW microwave resonators with aluminium films, fabricated on LAO and MAO substrates. Apart from the substrate preperation procedures, the fabrication process is identical for the MAO and LAO chips.

4.1 Substrate preparation

Preparation of an atomically flat, inert and uniform substrate surfaces have been shown to significantly decrease resonator losses in the quantum regime when compared with unprepared surfaces [1, 22, 29, 30]. In this section we describe the experimental methods used for surface preparation of our ternary metal oxide (TMO) substrates, LAO and MAO. Our methods for surface preparation consisted primarily of high-temperature annealing in controlled atmospheres, and ultrasonic agitation cleaning with acetone, isopropyl alcohol (IPA) and deionised (DI) water. The goal of the surface preperation phase is to prepare the potentially dirty and disordered as-received surfaces as contaminant-free, ordered and atomically flat surfaces. Our surface preperation includes the following general steps, the parameters of which are slightly adjusted for MAO and LAO. Note that no acid cleans are included due to the safety restrictions on the usage of acids by Honours students.

1. **Initial clean (acetone, IPA, DI water):** removes dust particles and other contaminants from the top of the surface

2. **Dry (nitrogen gas):** removes solvents and any additional contaminants collected during transportation

3. **Anneal:** surface reconstruction to produce a more uniform, atomically flat surface

4. **Final clean (DI water) and dry (nitrogen gas):** dissolves additional components and removes additional contaminants

4.1.1 Pre-anneal clean

Before annealing, we clean the substrate surfaces, with the goal of removing any surface contaminants left behind by the manufacturing process, or gathered during transport. This clean consists of sequential 5 minute ultrasonic agitations in VLSI (very large scale integration) grade isopropyl alcohol (IPA), acetone and Milli-Q DI water (in that order). To ensure that no residuals are left by the cleaning process, it is important to ensure that the wafer is quickly moved from IPA to acetone, and acetone to DI water. If the wafer is allowed to dry before being submerged in the next solution residuals may be left on the surface. Each of the sonication cleans were performed in dedicated beakers, which were thouroughly cleaned with IPA and rinsed with DI water before use. After the DI water sonication, the wafers were dried with nitrogen gas. Again, this should be done immediately after removing the wafer from the DI water. After the wafer is dried, it can be loaded into the tube furnace for annealing.

4.1.2 Tube furnace annealing

Annealing is a thermal treatment process used to alter the physical and chemical properties of a material [13]. It is a highly accessible technique used often in industrial applications, for example to increase the durability of steel. The annealing process consists of controlled heating of a material to a pre-determined temperature, sustaining this temperature for a pre-determined time period in a controlled atmosphere, then cooling the material back to a resting temperature. The exact effects of annealing depend on material, temperature, heating rate and atmosphere. In the context of our research, annealing can decrease substrate roughness, improve surface termination (i.e. by removal of loose-hanging bonds, which are known to be a source of TLS), and create a more structured and uniform surface, ideal for nucleation during film growth [13, 58, 59, 65, 108, 128, 129]. As the material is heated to annealing temperatures, the surface layers of atoms can diffuse into a more desirable configuration, a process known as surface reconstruction. This process is visualised in figure 4.1. For example, an as-recieved LAO substrate could have islands of LaO and AlO_2 randomly distributed across the surface (figure 4.1a). The annealing process would allow these regions to join and/or move in order to create a more structured surface (figure 4.1c). Kamal et al. [58] showed that devices fabricated on annealed substrates can produce Q-factors an order of magnitude higher than identical devices fabricated on non-annealed substrates.

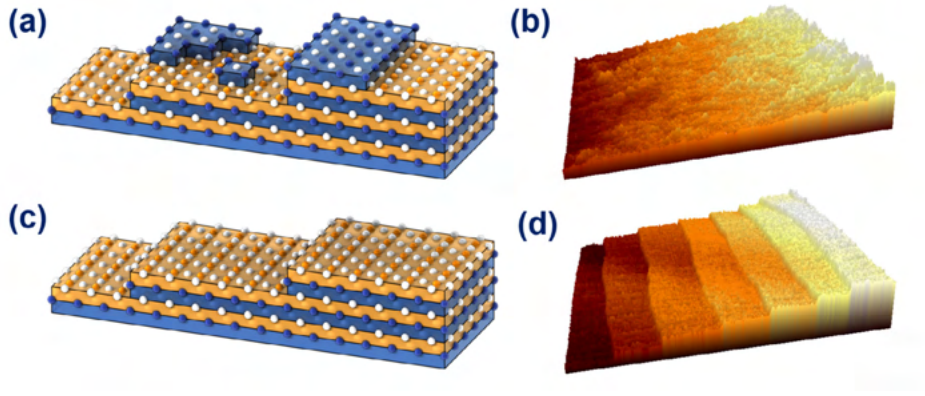


FIGURE 4.1: Simulated atomic structure and equivalent AFM topography of: **a-b)** an as-received substrate and **c-d)** an atomically flat surface, as created by annealing. Figure taken from Refs. [13] and [14].

For our fabrication, we used a Nabertherm tube furnace with Nabertherm B410 controller for annealing, located at ANFF-Q on the UQ Long Pocket campus. This furnace has a maximum operating temperature of 1200°C, and a ceramic tube diameter of 50 mm (tube model Nabertherm C 530). The ceramic tube has a maximum heating rate of $3.3\text{K}\,\text{min}^{-1}$, which sets a limit on the maximum safe heating rate. A manually-controlled flow of O_2 or N_2 can be fed into the furnace, or it can be closed and pumped to a vacuum ($P \sim 10^{-4}$mbar) during annealing.

LAO anneal recipe

Kim et al. [108] studied surface preperation of LAO with annealing, finding that annealing produced a drastic change on the surface. A well ordered, uniform terrace structure is formed, and surface roughness decreases after annealing. These step sizes were found to be on the order of the primitive lattice constant for LAO, meaning that each terrace steps down by a whole crystal cell, leaving the surface termination uniform across all terraces. Multiple annealing recipes were tested, and the most effective was found to be a 3 hour anneal in a tube furnace at 1200°C in an O_2 flow of $0.5\text{l}\,\text{min}^{-1}$ [108]. Due to the success of this recipe, and our ability to reproduce it perfectly with accessible instrumentation, we used this recipe for our surface preparation of LAO, finding results that agree strongly with those published in Ref. [108]. Other studies, such as those by Gunnarsson et al. [128] and Biswas et al. [13], have also shown the effectiveness of high temperature annealing on LAO using similar parameters to the recipe developed by Kim et al. [108].

MAO anneal recipe

An in-depth study on the effects of annealing temperature and conditions on MAO surfaces was performed by Jensen et al. [129]. The preferred method discussed by Jensen [129] includes a high temperature tube furnace anneal at 1100°C for 5 hours in air. This initial anneal is then followed by multiple cycles of sequential high-temperature flash annealing (at

temperatures from $1100-1200$°C for 10 minutes in O_2) and argon sputtering (1000eV Argon ion energy) in a UHV chamber. Due to experimental constraints, we could not perform the UHV surface treatment. Instead, we combine elements of Jensen's recipe, and anneal our substrate at 1100°C for 5 hours in O_2 at a flow rate of $0.5\mathrm{l\,min^{-1}}$.

Tube furnace operating principles

A full annealing cycle in a tube furnace will normally take between 12 and 24 hours (assuming the maximum temperature is sustained for 3-10 hours). Before loading samples into the furnace, the desired recipe (such as the one shown in figure 4.2c) must be programmed into the furnace controller. This is generally done in segments. For example, segment 1 is the ramp up from room temperature to the desired annealing temperature, segment 2 tells the furnace how long to stay at the annealing temperature, and segment 3 is the cool down to room temperature.

Once the recipe is programmed, the end cap from one end of the sample tube is removed for sample loading. The sample is then placed in a Alumina furnace boat (see figure 4.2b), which is pushed into the middle of the tube (where the desired temperature is reached) with a long metal rod. The rod should be marker so that the user knows when their sample is positioned in the middle of the tube. Both the metal rod and the furnace boat should be cleaned with IPA before use. The end cap can then be reattached. The contents and flow rate of the annealing atmosphere should then be set. In the setup used for this fabrication, oxygen or nitrogen gas (or a mixture of both) was available to be fed directly into the tube furnace, with their flow rates controlled manually. The water-cooling circulator should also be switched on before the recipe is started. Once all parameters are set, the recipe can be started. After the annealing cycle is complete, the end cap is removed and the furnace boat is carefully slid out of the tube with the metal rod. Any gas flow should be terminated upon completion of the recipe.

4.1.3 Post-anneal clean

In the case of LAO, we do a 120 minute ultrasonic post-anneal clean in DI water, a process referred to as DI water leaching in the literature. The DI water was initially at 27°C, and increased in temperature to 65°C over the course of leaching. This method of sequential annealing and DI water leaching was devised by Kim et al. [108]. The DI leaching process gradually removes LaO components from the surface, leaving the LAO surface with primarily AlO_2 termination [108]. By removing the LaO components, we are left with a more uniform surface structure suitable for defect-free film growth. Our post-anneal clean of the MAO chip simply consists of a 5 minute ultrasonic clean in DI water. This clean was chosen to remove any surface contaminants without altering the chemical or topographical structure of the MAO surface. Both wafer were dried with Nitrogen gas after their respective cleaning processes.

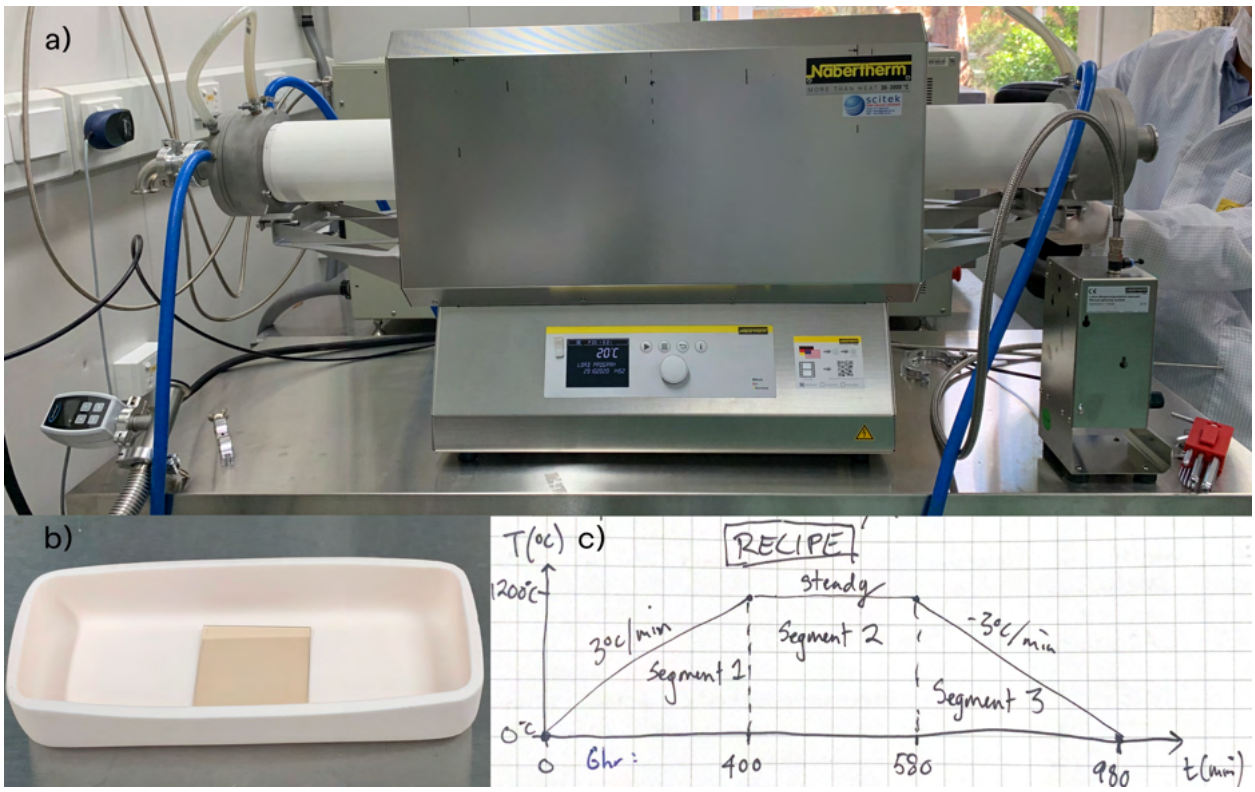


FIGURE 4.2: **a)** Nabertherm compact tube furnace with B410 controller. The furnace has a maximum operating temperature of 1200°C, and a maximum heating rate of 3.3K min^{-1} set by the maximum safe heating rate of the ceramic tube. The sample tube has a diameter of 50mm. The blue pipes, linked to a chilled water supply, circulate cold water around the furnace so it is safe to touch after operation. The metal box on the bottom right is used to control the gas flow rate into the tube. **b)** A 25.4 x 25.4mm LAO substrate sitting in a Alumina combustion boat purchased from Sigma-Aldrich. The substrate was just removed from the furnace after an annealing run. **c)** The recipe used for the LAO anneal cycle. This recipe was directly programmed into the B410 furnace controller.

4.2 Film deposition

Film deposition was performed in a PLASSYS MEB550S electron-beam (E-beam) evaporator (see figure 4.3b). E-beam evaporation, or E-beam physical vapour deposition, is a method of physical vapour deposition commonly used for thin film growth. Here we discuss the general operating principles and the deposition recipe used in this experiment. A graphical representation of the operating principles is shown in figure 4.3a. We used E-beam evaporation to deposit 100nm aluminium films at 0.5nm/s in a high vacuum environment.

4.2.1 Sample loading and preperation

Before loading the wafers into the load lock chamber of the PLASSYS MEB550S, the chamber must be vented to atmospheric pressure. This is an automated process in which the load lock chamber is pumped with nitrogen gas to increase its pressure. Once the chamber

is pressurised, the prepared substrates are secured to the sample holder, and placed back in the load lock chamber. The standard sample holder in the PLASSYS evaporator can support chip sizes up to 25.4 × 25.4mm. Whilst the load lock is pressurised to atmosphere, the user should also ensure the crucibles are stocked with deposition materials. The chamber then needs to be pumped down to operating pressure, which in our case is from 1×10^{-8}mbar to 1×10^{-7}mbar (high vacuum). The pump-down procedure takes about 48 hours. A film deposited in lower pressure will generally have fewer defects due to environmental interference. For the nanofabrication of high-Q devices, films should be deposited in high vacuum or lower pressures.

4.2.2 Deposition parameters

E-beam deposition in a PLASSYS evaporator is a very automated process. The user has control over the deposition material, rate and total thickness, and sample orientation relative to the source crucible. Since our circuits are planar devices, the sample remains orientated at 90° to the crucible's line-of-sight for the duration of deposition. For more complex designs, such as Josephson junctions fabricated by shadow evaporation, the sample orientation is a key parameter in the process [86].

The E-beam deposition rate has been shown to impact the grain size and surface roughness of polycrystalline aluminium films [130]. An increased deposition rate will result in larger grains and a rougher surface, whilst a slower rate produces a smoother surface with smaller grains (tested with deposition rates from 0.1nm/s to 2.0nm/s). As grain boundaries are likely to host a high density of TLS, we do not want to simply minimise roughness. We use a deposition rate of 0.5nm/s to achieve a balance between surface smoothness and grain size. We found that deposition at this rate produced grains with a median size of 34nm. In practice, the deposition rate is controlled by adjusting the current flowing through the tungsten filament from which the electrons are ejected; a larger current corresponds to a faster deposition rate. The deposition rate and thickness is monitored by a Quartz Crystal Microbalance (QCM) system in the load lock chamber, which is located near the substrate's position during deposition. The key component of this system is a mechanical cantilever oscillator, with a resonant frequency f. As more mass is deposited onto the cantilever, its resonant frequency will shift. Accounting for the atomic mass of the deposited material, the shift in frequency can be used to calculate the deposition thickness. The QCM systems used in E-beam evaporators generally guarantee precision within 2nm. With x-ray reflectivity measurements, we were able to confirm that the true film thickness matches with the QCM-measured thickness within 2nm. Once the deposition process is complete, the load lock chamber again needs to be pressurised to atmosphere before unloading the samples.

4.3 Chip design

We design notch-port transmission line (TL) coupled CPW resonator circuits on 2.1 × 7.1mm chips. On each chip, there are 5 resonators with natural frequencies f_0 from 4 - 8GHz, with the resonators decreasing in frequency from left to right along the transmission line. We fabricate several of these chips (and some other test structures) on a single wafer,

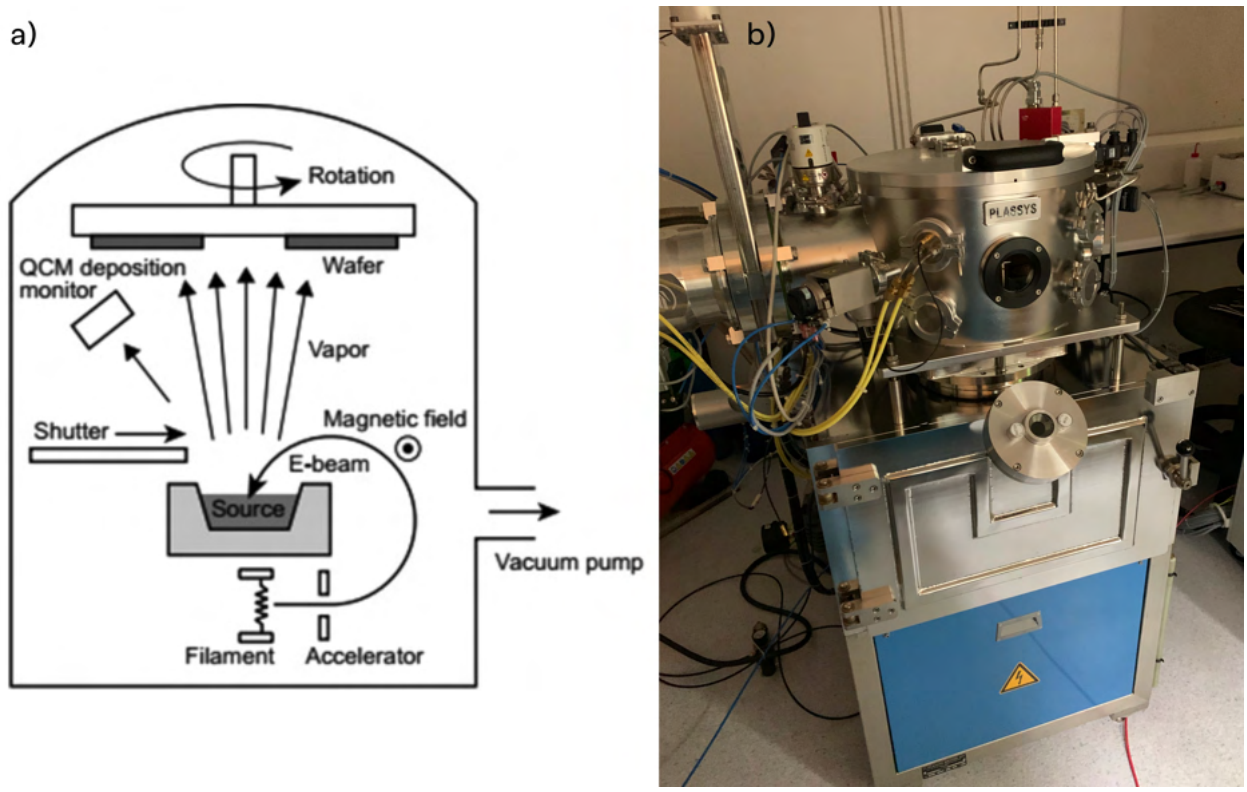


FIGURE 4.3: Panel **a)** shows a graphical representation of the operating principles of E-beam evaporation. A large current is passed through a tungsten filament from which electrons are ejected. These electrons are then steered and accelerated by magnetic (or electric) fields towards a crucible containing the material to be evaporated. The high energy electrons cause the material to transition to a gaseous phase, resulting in evaporation. The evaporated particles then travel through the high-vacuum ($P \approx 2e-8$mbar) chamber, coating everything (including our wafer) within line-of-sight of the source crucible. The PLASSYS MEB550S E-beam evaporator used for our film deposition is pictured in **b)**.

as shown in figure 4.4. The circuit elements and resonator-TL coupling scheme are discussed in section 2.1.2 and visualised in figure 2.1. We use `klayout` software to design the circuits, which we export in `.gds` files which can be input directly to the direct-write laser lithography system discussed in section 4.4.2. An example script with ample commenting is attached in appendix A.1.The resonators were adapted from a design provided by Eric He (SQD Lab), which utilises a specialised superconducting quantum hardware design package for `klayout`'s python implementation. This package was collaboratively developed by various members of SQD Lab. In this section, we explore the considerations that must be made when designing the geometry of resonator features, and how they are impacted by material properties.

4.3.1 Geometry and impedance matching

A well-designed TL-coupled CPW resonator circuit should be impedance matched at the input and output ports of the chip. This ensures that the power transfer from the external

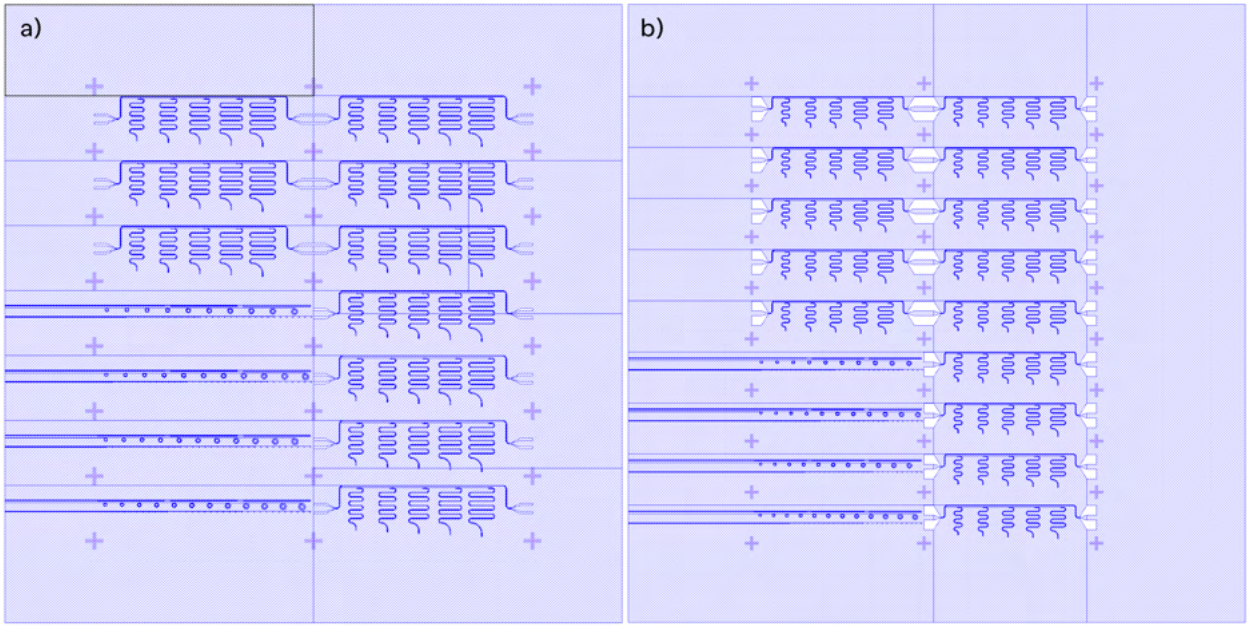


Figure 4.4: Circuit layout and design for resonator chips on: **a)** MAO substrate (20mm x 20mm), and **b)** LAO substrate (25.4mm × 25.4mm). The design was made on klayout using a Python code adapted from Eric He (SQD Lab at UQ). The crosses mark the individual circuit borders, and are used as indicators for dicing. Each individual circuit is 2.1mm × 7.1mm in size. The four circuits in the bottom left of either chip are non-functional 'test' circuits that are used only for characterisation. All the other circuits are TL-coupled $\lambda/4$ SCPW resonators. Each circuit contains five resonators with frequencies from $4 - 8$GHz. The highest frequency (shortest total length) resonator is the left-most resonator in each circuit. Note that the horizontal lines are artefacts of the klayout software, and are not part of the lithographed design.

PCB's feedline to the resonator chip's transmission line (and vice-versa) is maximised. In the case of an input or output that is not impedance matched, some proportion of the signal would be reflected at this point of the circuit. This will result in: less power being transferred into (and/or out of) the resonator circuit (difficult to account for) [15, 87]; standing waves on the resonator circuit's transmission line due to reflections at the input and output [5, 22]; phase and amplitude errors [87]; and a reduced signal to noise ratio [87]. Experimentally, all of these effects make for a more difficult and potentially inaccurate measurement of the S_{21} transmission through the chip. A resonator that is perfectly impedance matched should have a $|S_{21}|$ resonance very close to an ideal Lorentzian in shape (corresponding to a circular resonance in the complex S_{21} plane), as described in section 2.1.5.

In our case, we want the input and output impedance to be matched at $Z = 50\Omega$ as this is the impedance of the feedline on the PCB to which the chip's feedline is wire-bonded (see section 4.6). This is a common characteristic impedance used in microwave circuits [15, 87]. For complex microwave systems, numerical simulations are often used to ensure impedance matching and intended functionality, however in the case of TL-coupled CPW resonators, analytical solutions are possible. A full analytical derivation of the electromagnetic behaviour of a CPW resonator weakly coupled to a CPW transmission line is given

by Besedin et al. [15]. The technique of conformal mapping (originally used by Wen [36] in his 1969 paper proposing the CPW resonator structure) is used to construct a solvable system of equations describing the coupled TL and resonator system. We use this theoretical description, implemented through the accompanying web tool, to ensure that our devices are well impedance matched. This tool is also used to calculate the first order coupling correction to the resonant frequency of the resonators, which is a correction on the order of MHz to the natural frequency given in equation 2.9. An example use of Besedin's web tool is shown in figure 4.5.

The characteristic impedance, coupling strength and resonance frequency of these devices are heavily impacted by the dielectric constant ϵ_r of the structure's substrate. A device made with a high dielectric constant substrate will require larger gap (S) dimensions to achieve the same coupling behaviour as a device with a low dielectric constant substrate. This is due to the dependence of field lines and density on the dielectric constant of the medium through which the field is propagating. Furthermore, the natural resonance frequency of the resonators is dependent on ϵ_r (see equation 2.9); the length of the resonators is also dependent on the material choice. A material with a high dielectric constant will have a shorter resonator than a material with a lower dielectric constant at the same resonance frequency. In our case, MAO has a room temperature dielectric constant $\epsilon_{\mathrm{MAO}} = 8.325$ [72] in the microwave regime, and LAO $\epsilon_{\mathrm{LAO}} \approx 25$ [65]. For comparison, silicon has a microwave dielectric constant of $\epsilon_{\mathrm{Si}} = 11.6$ at room temperature ($T = 300\mathrm{K}$) [131], a value sitting in between those of LAO and MAO. All of these materials are non-magnetic, with $\mu_r \approx 1$. Due to the differences in dielectric constant, device made on all three materials will have varying dimensions.

In order to compare our test chip with a previously fabricated Al on Si CPW resonator, we kept the sum of $2W + S$ constant across all devices (the total width of a transmission line, or resonator line). The Al on Si has $S = 8\mu\mathrm{m}$ and $W = 14\mu\mathrm{m}$, so $2W + S = 30\mu\mathrm{m}$. This means the LAO device (higher dielectric constant) will have a smaller central conductor width W, and a larger gap width W, and vice-versa for the MAO chip. The gap/width dimension for LAO are $S = 12\mu\mathrm{m}$ and $W = 6\mu\mathrm{m}$ ($S/W = 2$), and for MAO, $S = 6\mu\mathrm{m}$ and $W = 18\mu\mathrm{m}$ ($S/W = 1/3$). As discussed, the gap/width ratio differs due to the difference in dielectric constant between the two materials. The LAO (high dielectric constant) chip has a larger SA (substrate-air) interface, and smaller SM (substrate-metal) and MA (metal-air) interface areas than the MAO chip. Previous studies on resonator geometry have shown that circuits with larger dimensions perform better in the single photon regime due to a lower field density on surfaces and interfaces [46]. It is currently not agreed on in the literature which interface hosts the highest density of TLS [1], however if this was determined it would make one class of material (high or low dielectric constant) more appealing due to the ratio of interface areas.

4.3.2 Practical design considerations

In addition to the material-based design considerations, there are other more practical factors that must be accounted for when designing the chip. We must ensure that the contact pads on the input and output of the transmission line are large enough for wire bonding. Ideally,

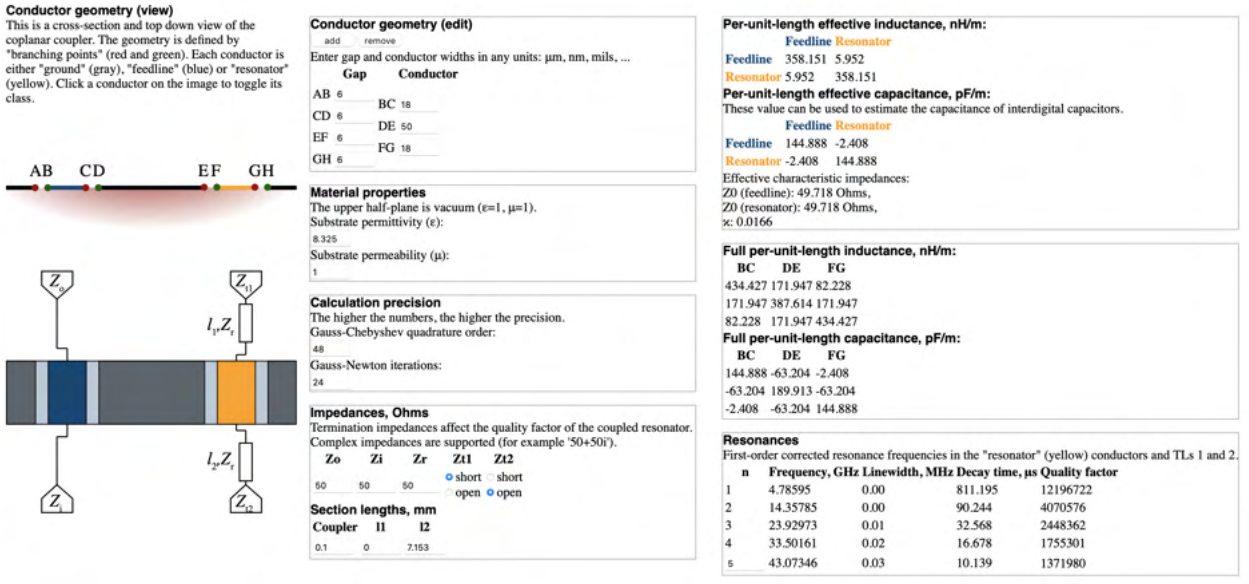


Figure 4.5: Example usage of the web tool developed by Besedin et al. [15] for calculation of TL-resonator coupling strength κ (dimensionless parameter), transmission line (blue) and resonator (yellow) impedances Z_0, and corrected resonance frequencies on the MAO ($\epsilon = 8.325$) chip. The program takes inputs of the relative permittivity and permeability (ϵ_r and μ_r respectively) of the substrate, gap S and conductor widths W (transmission line, coupling distance, and resonator), coupler length, shorted and open lengths of the resonator (l_1 and l_2 respectively), and input, output and resonator impedances (Z_i, Z_o and Z_r respectively). In our case, all chips were designed with the shorted end in terminating the coupling region, hence $l_1 = 0$. The web-tool is also able to simulate the resonator's lossless (ideal) Q-factor.

we would have at least two wire bonds connecting the chip to its external measurement circuit. As discussed in section 4.6, each bond requires about 100µm linearly. Therefore the contact pad should have a width and length of at least 200µm. In our case, the contact pads were designed to be 200 × 400µm to allow for some human error in the wire bonding process.

It is also important to ensure that the circuit features do not come within 100µm of the chip's border. This is to allow for the non-zero thickness of cuts applied during the dicing process. Features closer to the edge than this would run the risk of being cut into during dicing. Furthermore, unintended coupling should be avoided by ensuring that separate circuit elements are not placed too close together.

Finally, it is advantageous to place structures in the middle of the wafer, as the spin coating, and therefore all lithography steps, are more uniform here. This is due to boundary-effects causing a small amount of resist build-up around the edges. This build up can result in uneven exposure towards the edges of the chip (see figure 4.7d). This is discussed in section 4.4.

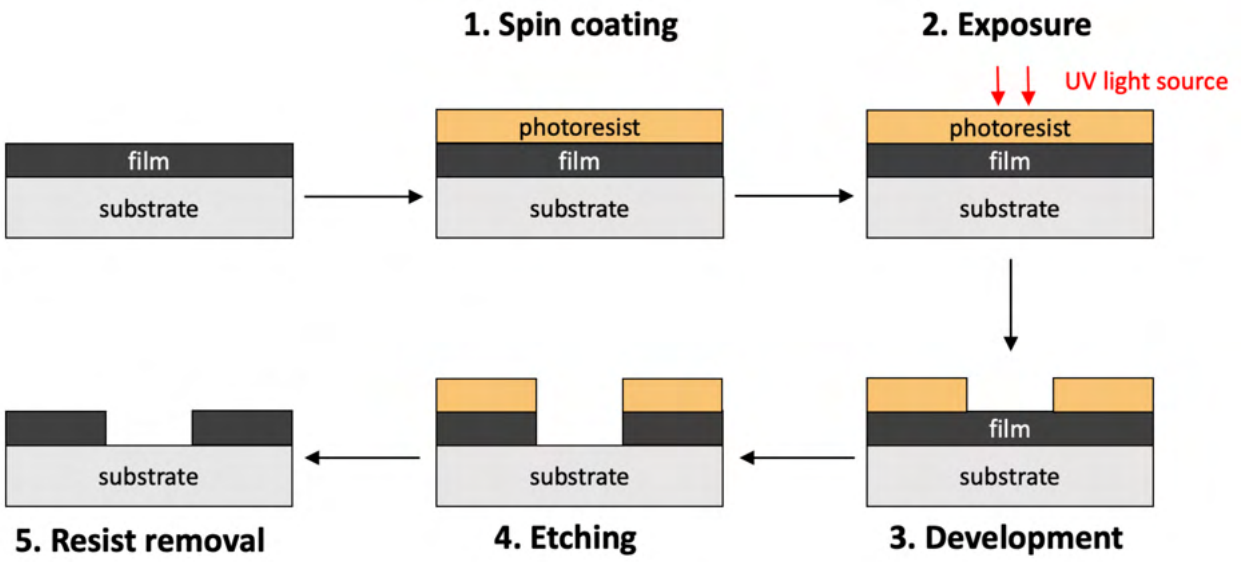


FIGURE 4.6: An overview of a direct-write optical lithography process using positive photoresist.

4.4 Direct-write laser lithography

Here we discuss the lithography process, which is used to pattern the designs shown in figure 4.4 into the devices' aluminium films. In our fabrication, we use direct-write optical lithography, which refers to the exposure step of the lithography process. This method has a minimum resolution of around 2µm, which is sufficient for our designs. If a smaller resolution is required, electron-beam lithography is generally used, which can pattern sub-10nm structures [132]. Lithography was done in collaboration with Eric He of SQD lab.

The lithography process is broken into multiple steps, as shown in figure 4.6. First, the film is coated with a light-sensitive material called photoresist. The device structure (provided as a digital `.gds` file) is then directly exposed into the photoresist. In the case of positive photoresist, the exposed areas of the photoresist can be removed by a special developer chemical. This then leaves the film exposed only in the areas where it will be removed. At this stage, a metal etchant is used to remove the exposed film. Finally, the remaining photoresist is removed with solvents.

4.4.1 Spin coating

Spin coating is the first step of a direct-write lithography process, and refers to the application of a uniform layer of light sensitive photoresist on top of an existing structure. Lithography as a whole is very sensitive to the thickness of the photoresist layer. For example, if the resist is too thick, the pattern will be underexposed and the structure will not be properly resolved by development. An example of an underdeveloped structure is pictured in figure 4.7e. The opposite effect can occur if the photoresist layer is too thin, as shown in figure 4.7c.

In the case of direct-write laser lithography, the photoresist is coated on top of the Al film. We use a Sawatec SM-200 spin coating module, located in the ANFF-Q class

10000 cleanroom, to perform spin coating. The Sawatec system has inbuilt resist dispensing, however we manually dispense resist for more control over the storage conditions for the photoresist. We use AZ1512-HS positive photoresist, which has a high contrast allowing for relatively fast development times. This resist should be stored at 0°C, however should be at room temperature for usage. For this reason, we remove the photoresist from its storage fridge at least 12 hours before usage.

To achieve a uniform, controlled photoresist coating, the wafer is rotated at a large RPM. The viscosity of the chosen photoresist, and duration and speed of the rotation determine the thickness of the photoresist layer. In the case of spin coating with the Sawatec SM-200, the parameters must be programmed into the instrument controller before starting the recipe. Our recipe reaches a maximum rotation speed of 5800RPM for a duration of 60 seconds. Using a Bruker Dektak stylus profiler, we were able to confirm that this recipe produces a photoresist thickness of 1.3 ± 0.2µm. The variation in the thickness is due to the dependence of the photoresist viscosity on temperature and humidity [132].

To perform spin coating, the wafer is first secured to a sample holder chuck with vacuum. We use a rubber o-ring around the chuck to improve adhesion, which is especially important in the case of rougher wafers. We then manually dispense approximately 30ml of AX1512-HS resist on to the centre of the wafer and start the programmed recipe (5800RPM for 60 seconds). Once the process is complete, the vacuum is disengaged, and the sample is removed from the chuck immediately on to a metal hotplate at 110°C for 60 seconds. This process is called a softbake, and is used to improve adhesion between the photoresist and underlying material. Note that it is important to ensure the wafer is free of contaminants before spin coating, as any particles trapped under the photoresist layer will negatively effect the lithography process, and could result in short-circuiting or unresolved structures.

4.4.2 Exposure

After spin coating and the softbake, the chip is ready for exposure. We use a Heidelberg Instruments μPG101 desktop laser write system to expose our designs into the photoresist layer. This system uses a diode laser at $\lambda = 405$nm to expose the designs. For our chosen photoresist (AZ1512-HS) and thickness (1.3 ± 0.2µm), we set the laser power to 45mW, with 25% intensity. Decreasing the laser power would result in an underexposed structure and vice-versa.

To initiate the exposure process, we load the sample and secure it with the μPG101 system's built in vacuum. The sample is then aligned, and the laser focus is calibrated using the Heidelberg Instruments Exposure Wizard software. Once aligned, the design can be digitally loaded into the Exposure Wizard software in the form of a `.gds` file. The laser power and intensity is set, and the process is initiated. This system takes approximately 5 hours to expose the designs shown in figure 4.4. After the exposure is complete, the wafer is placed on a metal hotplate at 90°C for 60 seconds. This is referred to as a post-exposure bake, and helps solidify the exposed structure. It is very important that the photoresist is not exposed to any additional light source between the end of exposure and start of development.

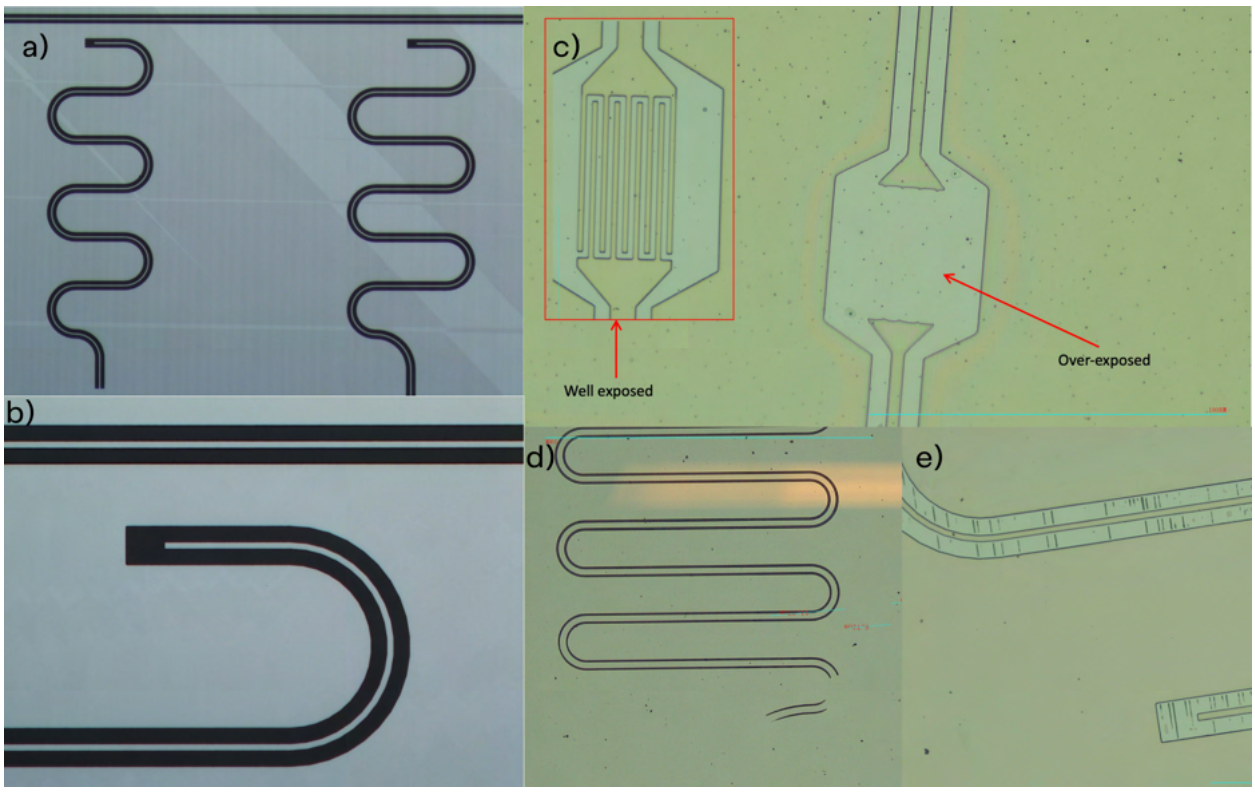


FIGURE 4.7: Optical microscope photos at multiple stages of the lithography process. Panels **a)** and **b)** show successful lithography on the LAO chip. The images were taken after etching and resist removal. Images **c)**, **d)** and **e)** show potential issues that could arise during lithography. In panel b), we see an example of overexposure due to the photoresist layer being too thin for the chosen exposure power (or conversely, the exposure power being too large for the resist thickness). Image d) shows the effects of the edge-bead problem that arises during spin coating. We see uneven exposure due to a non-uniform photoresist thickness near the edge of the chips. Finally, panel e) shows an example of underexposure, where the direct-write laser was not able to provide enough power to fully expose the structures. The stripes are an artefact of the laser's raster path during the writing process.

4.4.3 Development

In the case of positive photoresist (as used in our fabrication), the development process removes exposed areas of photoresist. We use AZ726 metal ion free (MIF) developer to remove exposed AZ1512-HS. Development is a very time-sensitive process; leaving the chip submerged in developer for too long will result in over-development, where the intended structure is broadened due to the developer eating away at non-exposed areas of photoresist. We also observed that the developer can start to etch the aluminium film after ~ 60 seconds of submersion. An under-developed sample will have structures smaller than the intended geometry.

Before beginning the development, we thoroughly clean three beakers with VLSI (electronic grade) IPA and DI water. The first beaker is filled with AZ726 MIF developer, and the other two with fresh Milli-Q DI water. To develop our sample, we carefully grab the wafer

with non-magnetic tweezers and submerge it in the developer for exactly 50 seconds. While it is submerged, the wafer is shaken gently to ensure the developer resolves the smallest exposed structures. Immediately after the 45 seconds in developer the sample is sequentially submerged in the two DI water beakers for 15 seconds each, before being thoroughly dried with nitrogen gas. After the development is complete, the structure should be carefully examined under an optical microscope to check that all structures are completely developed, and the scale of structures matches the designs. If the scale does not match, it is likely that the sample was over- or under-exposed or developed. As we discussed in section 4.5, incorrect scales could result in impedance mis-match and/or unintended coupling.

4.4.4 Etching

The final step of the lithography process is etching, in which the areas of exposed film are removed by a wet metal etchant. Dry etching processes also exist, however were not possible for our project due to safety restrictions. We use an aluminium etchant that contains 21% DI water, 73% phosphoric acid, 3% acetic acid, and 3% nitric acid. The etchant was mixed by Eric He of SQD lab.

Similar to the development process, the wafer is submerged in the etchant for a period of time, before being rinsed sequentially in high purity water and DI water. We therefore prepare these three beakers before beginning the etching process. In general, the etch time will vary from sample to sample. Devices with smaller scale structures will require a longer etch time than an equivalent sample with larger scale structures. This is because the etchant is able to act more efficiently on larger areas. We found that the larger exposed areas (such as the gap around the contact pads - see figure 4.4) were etched more quickly than smaller areas such as the transmission line gap. This is one disadvantage of wet etching; it can be difficult to get even etching across all on-chip structures. To find the optimal etching time for our structures, we etched our test chips for 10 seconds at a time, before rinsing them in the water beakers and checking the etching results by optical microscopy. Once the etching looked close to complete, we etched in 5 second intervals. We found that the structures were fully etched after 35 seconds.

To etch our films, we submerge the wafer into the aluminium etchant for 35 seconds, before sequentially submerging it in the pure water and the DI water. Similar to the development process, the structures should be viewed by optical microscopy to check for uniform etching and correctly resolved structures. Once the etching is satisfactory, the remaining photoresist can be removed by a 2 minute submersion in 60°C VLSI acetone, followed by a 15 second rinse in VLSI IPA. The wafer is then dried with nitrogen gas. Whilst it would be more efficient to remove the resist by sonicating the chip in acetone, we found that this could damage the film, causing areas to become chipped or cracked. Another suggested method of photoresist removal is via supercritical CO_2 drying [112], however we were not able to try this method.

4.5 Dicing

After the resonator circuits have been lithographically patterned into the aluminium film, the individual circuits shown in figure 4.4 must be diced. There are 14 separate 2.1mm x 7.1mm circuits on the MAO wafer, and 18 on LAO. When devices are diced after being patterned, the process is referred to as post-dicing. Once diced and cleaned, the wafers are ready to be seated and wire-bonded to a PCB, as discussed in section 4.6.

4.5.1 Protective photoresist layer

Before dicing, the wafer should be spin coated with a layer of photoresist. This acts as a protective layer on top of the aluminium film, preventing the surface of the device from being exposed to dust during dicing. The protective layer also prevents the dicing blade from cutting into the aluminium film directly, as this would be more likely to result in the film cracking. Since the spin-coat is only protective, there is a low sensitivity to thickness; a photoresist thickness between 1 and 2µm is satisfactory. The protective spin-coat was done using the Sawatec SM-200 spin-coating module located at the Australian National Fabrication Facility (ANFF-Q) [19]. We used the recipe detailed in section 4.4.1 to coat the device surfaces with a protective layer of 1.5µm AZ 1512 HS photoresist [133].

4.5.2 Dicing recipe: cutting parameters and blade choice

An ADT 7100 precision dicing saw located at ANFF-Q was used for dicing. Different materials require specially configured dicing parameters and blades. When designing a dicing recipe, an important mechanical property to consider is the Mohs hardness of the substrate and the blade; the blade should always be harder than the material it is cutting through. For example, attempting to dice sapphire (hardness of 9.0 Mohs [134]) with a nickel (hardness of 4.0 Mohs [135]) blade will result in a snapped blade and a ruined substrate. Successfully dicing a sapphire substrate would require a much harder blade. MAO has a hardness of 8.0 Mohs [136, 137], and LAO has a hardness of 6.0 [138]. For comparison, silicon has a hardness of 6.5 Mohs [135]. In addition to blade choice, the spindle's RPM and linear cut speed can be set. We can also set the entry and exit cut speed, as the blade first makes contact with, and leaves the material. In general, a lower spindle speed will produce softer dicing action, and is therefore more suitable for fragile materials such as LAO. A lower spindle speed will however produce more wear on the blade, meaning that replacement blades will be required more often. One way to circumvent this issue is to decrease the cut depth, doing multiple passes for a cut through the full substrate depth. Decreasing the cut speed will increase the total duration of the dicing procedure, but there will be fewer strain forces on the substrate during dicing. A feed rate that is too high can produce excessive cracking and chipping.

Unsuccessful recipes

Finding the correct configuration for certain dicing conditions can often be a process of trial and error. We tested multiple blades and parameters before finding the most suitable configuration. We first attempted to dice LAO with a resin blade (ADT brand, model

number 00777-H020-010-QKP [17]) at 20KRPM and 2mm/s feed rate. As shown in figure 4.8e, these parameters resulting in excessive cracking, likely due to the spindle speed and feed rate being too high. We then swapped to a different resin blade (ADT brand, model number 007L7-1053-010-Z01 [17]) to dice the MAO, the results of which are shown in figure 4.8f. This blade did not result in cracking of the substrate, but upon removal from the dicing instrument, it was found that approximately half of the diced circuits were dislodged from the dicing tape during the process. These results proved the need for a more suitable recipe and blade.

Final Recipe

For convenience, we wanted to use the same blade to dice MAO and LAO, as well as sapphire (another commonly used substrate in SC quantum hardware with similar mechanical properties to MAO). We therefore require that the blade has a hardness greater than 9.0 Mohs, the hardness of sapphire. Our choice was therefore limited to a diamond blade; Microkerf Minitron brand, model number 2.187-8-45H (see figure 4.8c). To avoid the cracking and chipping that arose during the test runs, the spindle speed was reduced to 10KRPM, the cut speed to 0.5mm/s, and the entry and exit cut speed to 0.1mm/s. This could be considered a cautious recipe, however the results on MAO, LAO and sapphire are fantastic. The MAO and LAO wafers diced with this recipe are shown in figures 4.8a and 4.8b respectively. The dicing saw was operated by Eugene Sachkou, and the recipe was developed in collaboration with Wael Al Abdulla at ANFF-Q.

4.5.3 Sample loading and operation

As shown in figure 4.8d, samples are mounted onto Nitto silicon wafer tape SWT-R [16] attached to a metal frame for dicing. This is performed on the ADT WM-966 manual wafer mounter, which assists with sample alignment and heats the wafer tape, increasing the adhesion of the wafer to the tape. It is important to ensure no dust or air bubbles are present in between the wafer and tape to maximise adhesion. If the wafer is not well secured pieces can be lost during dicing (as shown in figure 4.8f).

After the sample is loaded into the dicing saw, the sample orientation, size and cut geometry must be calibrated. This is done using the lithographed dicing marks (seen as crosses in figure 4.4) for alignment. The exact size of each chip in the x and y must be known, as the dicing saw indexes the cuts according to these dimensions. The user should confirm each programmed cut individually using the connected microscope camera and dicing marks. Once the desired cutting parameters (spindle speed, cut speed) are also set, the recipe can be executed.

4.6 Wire bonding

The process of wire bonding is used to connect the diced chips to an external copper PCB. The PCB used in this experiment has two cavities, one for the MAO chip, and the other for LAO. The cavities are approximately 2.5mm x 7.5mm in size, and 0.5mm deep. Therefore,

the diced chips (approximately 7.0mm x 7.0mm) sit comfortably inside the cavity with a border gap of approximately 0.25mm around all edges. Since the MAO chip is 1.0mm thick, its surface sits about 0.5mm above the level of the PCB surface. To minimise chip movement during wire bonding and measurement, the chips are glued into the PCB cavities using poly(methyl methacrylate) (PMMA). Before gluing, the PCB was fully submerged in a citric acid solution for 10 minutes to remove the native oxide layer that accumulates over time. The PCB was then submerged in Acetone and IPA for a minute each, before being blow-dried with nitrogen gas. A thick oxide layer on the PCB would drastically decrease the success of wires to bond to the aluminium film during wire bonding. A small amount of glue was applied to the bottom of the PCB cavities before seating the chips in the cavities. The chips were left to dry for 20 minutes before attempting bonding.

To bond our chips, the TPT HB-16 Wedge and Ball Bonder [18] was used, located at ANFF-Q [19]. All wire bonding was done by Rohit Navarathna. We use cylindrical aluminium wire with a 33µm diameter. The HB-16 wire bonder uses ultrasonic vibrations, and the heat generated by these vibrations, to adhere the wire to the bonding surface. The bonder uses a 63.3kHz transducer PLL control for generate ultrasonic vibrations with 0-10W output power. In our case, the two bonding surfaces are aluminium (the thin film on our devices) and copper (the PCB). The HB-16 bonder allows for adjustment of force with which the bonding needle is pushed into the bonding surface whilst the needle is vibrated ultrasonically. Typically, this force is in the range of 100 - 500mN. The bond time can also be controlled. For our case, this was kept constant at 100ms across all surfaces. Finally, the *loop profile* of the bond can be programmed. This determines the path of the bonding needle after the first bond is made. Adjusting this path can result in more or less upward force on the initial bond location whilst the needle moves to the location of the second bond. It was found that a path which zig-zags from the location of the first to the second bond minimised the upward force on the first bond. Such a path alternates between upward and forward movements, travelling between 200-300µm per step. If the bonding parameters are not set optimally issues will arise, as detailed in table 4.2. In addition to these issues, there can also be wire-feeding issues if the feed mechanism is mis-aligned or blocked.

Issue	**Possible cause**	**Resolution**
Wires snapping at bonding points	Loop profile applies too much force on bond point	Reduce motor speed, adjust loop profile to zig-zag path
Bonding points lifting with film attached	Loop profile applies too much force on bond point	Reduce motor speed, adjust loop profile to zig-zag path
Bonds not adhering	Ultrasonic intensity is not high enough	Increase ultrasonic intensity

TABLE 4.2: Issues that arise during wire bonding on the TPT HB-16 Wedge and Ball Bonder [18]. A cause and resolution is presented for each issue. Note that these resolutions are applicable to 33µm aluminium wire bonded to aluminium or copper.

Ground plane connections, as well as input and output connections from the contact pads of the chip to the center conductors of the PCB are required. The ground plane connections

should mimic a plane, so ideally all points around the edge of the ground plane should be bonded to the ground plane of the PCB. In practice, this is not achievable due to the physical constraints of wire bonding; each bond takes up an area of approximately 80µm. The exact bond area is primarily dependent on the bonding force. Furthermore, attempting to place a bond overlapping a previous bond could result in damaging or removing the previous bond. As a result, the maximum bond density is approximately one bond per 100µm around the border of the chip. For this reason, we are able to fit two bonds from each contact pad of the chip to the PCB's central conductor, which act as the resonator's input and output lines. Due to the bond area, it is also important to ensure that there are no circuit elements less than 100µm inwards from the border of the chip. All bond lengths were minimised to reduce the distance of the impedance-mismatched region. A shorter bond-length will result in less attenuation, and better impedance matching from PCB to chip [87]. The minimum reliable bond length was found to be 500 ± 100µm. Figure 4.9 shows both the input and ground plane bonds on a portion of the chip. The image also contains a failed bond (enclosed in the red circle) in which the aluminium film was lifted under the bond location. This is an example of the second issue listed in table 4.2.

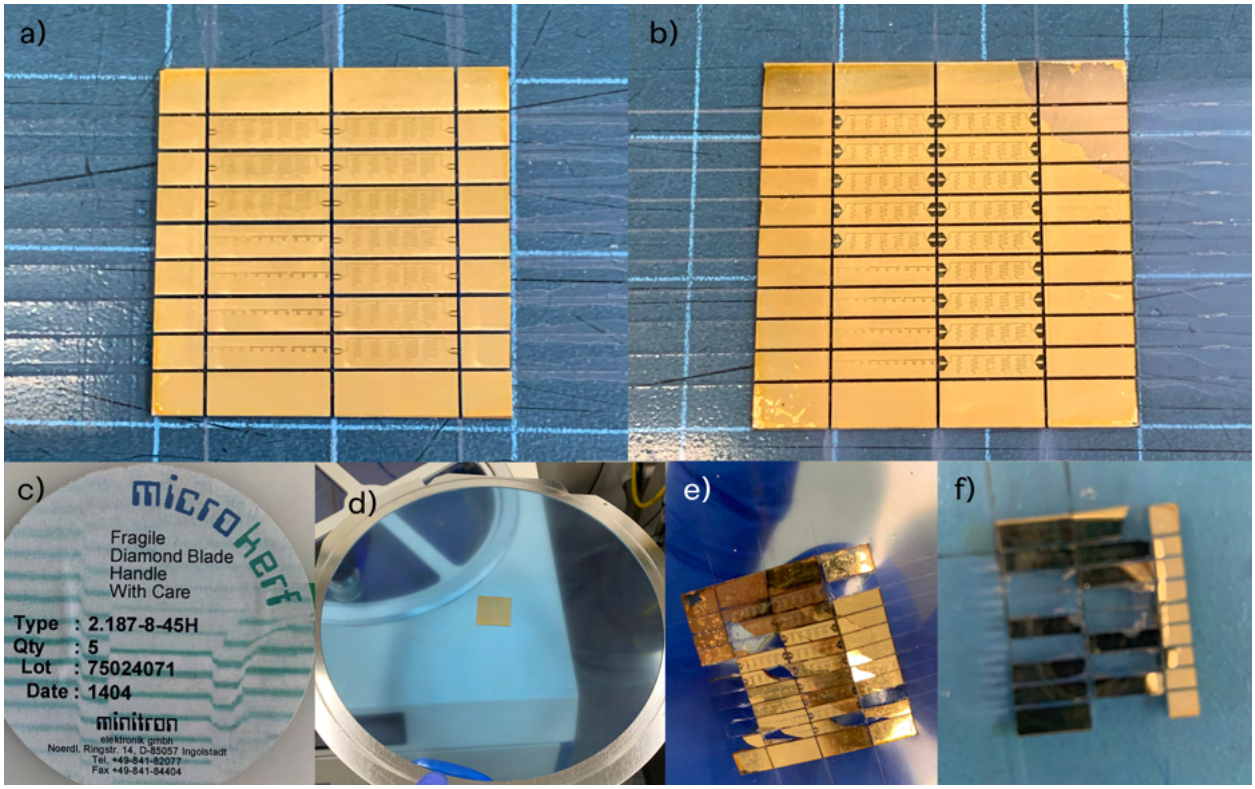


FIGURE 4.8: **a)** MAO wafer (as seen in figure 4.4a) and **b)** LAO wafer (as seen in figure 4.4b) after being successfully diced with the blade shown in e) at 10KRPM spindle speed, 0.1mm/s exit and entry speed, and 0.5mm/s cut speed. The silver section in the top right corner of the LAO chip (b) is due to the removal of resist during dicing. Both chips are mounted on dicing tape, photographed on top of a 1cm x 1cm grid board for scale. **c)** packaging for the Microkerf Minitron 2.187-8-45H diamond blades used to successfully dice LAO, MAO and sapphire. **d)** LAO wafer mounted on Nitto silicon wafer tape SWT-R [16], ready for loading into the dicing saw. **e)** LAO wafer after unsuccessful dicing with a resin blade (ADT 00777-H020-010-QKP [17]), and **f)** MAO wafer after unsuccessful dicing with a resin blade (ADT 007L7-1053-010-Z01 [17]) at 25KRPM spindle speed and 2mm/s cut speed. The yellow tinge on the wafers is due to the protective layer of photoresist.

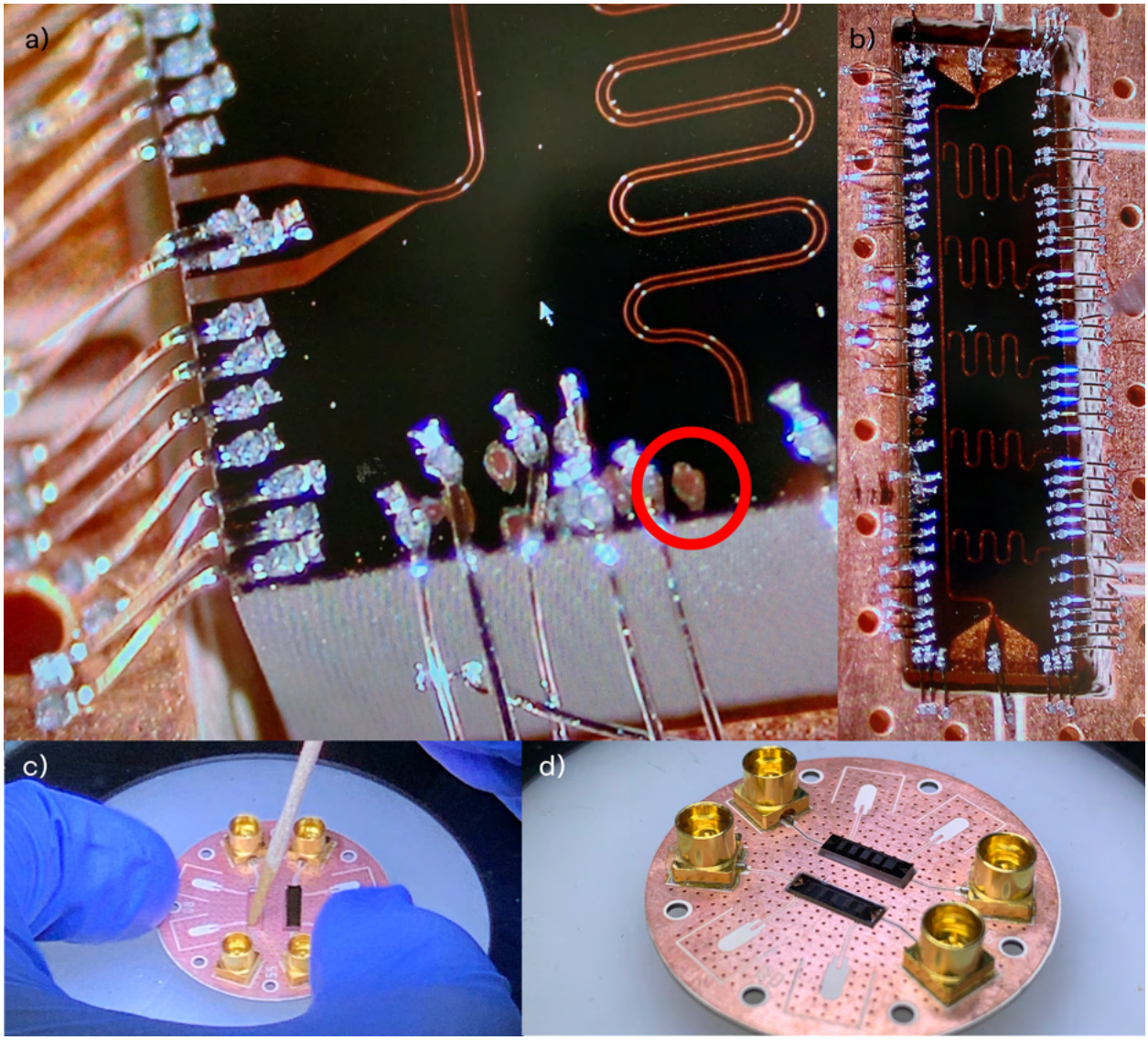


Figure 4.9: **a)** Ground plane and central conductor wire bonds on the MAO chip. A failed bond, in which the underlying aluminium film was lifted, is enclosed in the red circle. The two central conductor bonds can be seen on the left side of the image, where they are bonded to the contact pad of resonator circuit. **b)** The LAO chip after bonding. More failed bonds can be seen along the left-hand side of the LAO chip. **c)** PMMA being applied to the bottom of the second PCD cavity, where the LAO chip was seated, as shown in **d)**. The bonding was performed by Rohit Navarathna on the TPT HB-16 Wedge and Ball Bonder [18] at the Australian National Fabrication Facility, Queensland node (ANFF-Q) [19].

5 Device measurement setup

In this chapter we discuss the experimental setup of cryogenic S_{21} complex transmission measurements in the single photon regime. This includes discussions of sample shielding from external radiation and fields, sample mounting configurations to improve thermalisation, and measurement circuit setups to maximise the signal-to-noise ratio in the low power limit. All device measurements were performed in Assoc. Prof. Arkady Federov's lab.

5.1 Sample mounting and cooling

We use a Bluefors small dilution (SD) cryostat to cool our samples to the millikelvin range. The mixing chamber of the Bluefors SD reaches temperatures around 30mK, which is well within the quantum regime ($\hbar\omega_0 \ll k_B T$), and below the critical temperature of aluminium ($T_c = 1.2$K). These are the thermal conditions under which we want to measure our devices, so it is important to ensure the samples are thermally connected to the cryostat's mixing chamber. In general, the process of sample mounting includes: connecting the PCB to input and output lines, mounting the PCB in a copper cavity, attaching magnetic and radiation shielding, and thermally connecting the sample enclosure to the mixing chamber of the SD cryostat. For thermal connections, we use oxygen-free high thermal conductivity (OFHC) copper, which has great low-temperature thermal conductivity ($11000\,\mathrm{W\,m^{-1}}$ at $T = 20$K [139]). In our experiment, we only connected and measured one device at a time, as shown in figure 5.1c. Simultaneous measurement of both samples is possible with a cryogenic switch or voltage splitter, however this hardware was not available to us at the time of experiment.

In figure 5.1a, we see the PCB containing the LAO and MAO chips sitting on the bottom plate of an OFHC copper enclosure. The lid of this enclosure (shown attached in figure 5.1b) has two 1mm indentations where the samples sit. This ensures that the sample's SC film will not be in contact with the copper cavity. Furthermore, to ensure the no fields from the SC couple with the copper cavity, we require a considerable amount of vacuum between the film

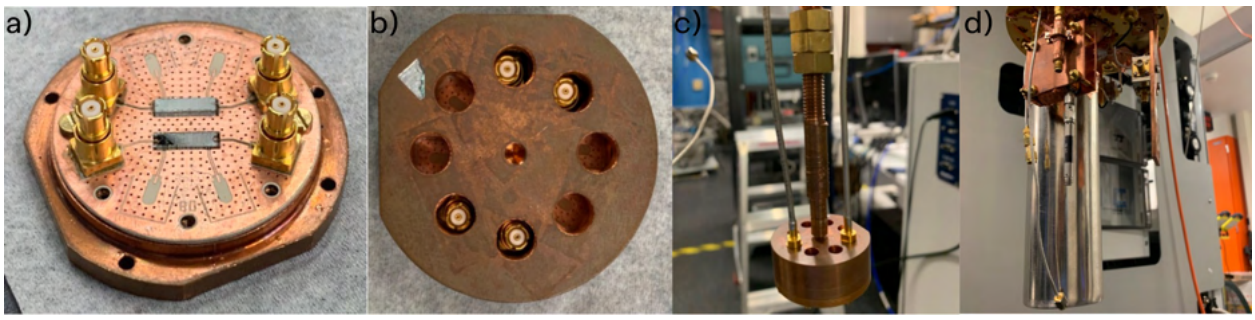


FIGURE 5.1: Sample mounting, connections, and shielding for measurements in a Bluefors SD refrigerator. Image **a)** shows the copper printed circuit board (PCB) containing the LAO and MAO resonator chips. The two ports on the left correspond to the input ports (port 1), and the two on the right to the output ports (port 2). Only one set of ports were connected at a time. In **b)**, we see the PCB fully enclosed in its oxygen-free high thermal conductivity (OFHC) copper cavity, which is aligned and fastened shut with brass screws. Image **c)** shows the OFHC copper cavity thermally connected to the mixing chamber of the dilution refrigerator by an OFHC copper 'cold finger'. In this image, we also see the input and output coaxial cables attached to the ports on the PCB, which are visible in a). Finally, in **d)** we see the outer layer of the Cryoperm 10 magnetic shielding enclosure, which is secured by brass screws to the 'cold finger'.

and copper surface. In the case of the MAO chip, which is 1mm thick, ∼0.5mm protrudes above the PCB surface, leaving 0.5mm of vacuum between the film and the copper cavity once the cavity lid is attached. The LAO chip is only 0.5mm thick, so approximately 1mm of vacuum lies between the film and cavity surface. In both cases, this is enough distance in vacuum to allow for the exponential decay of fields radiating outwards from the SC film.

Figure 5.1 shows the copper cavity attached to an OFHC copper 'cold finger', which is essentially a long screw that is attached to the cryostat's mixing chamber stage on the other end. This allows for thermalisation between the mixing chamber and the samples we are measuring. Usually, high thermal conductivity vacuum grease is used at the cold finger's connection with the mixing chamber to further improve heat transport. Vacuum grease was not used in our experiment.

To minimize non-TLS resonator losses due to quasiparticle excitations [140, 141] and stray magnetic fields [142], our samples are heavily shielded. We use three layers of Cryoperm 10 magnetic shielding, which is a high permeability material, optimised for near-absolute-zero temperature usage.

5.2 Principle of measurement

In this study, we measure the phase and amplitude of microwave signals transmitted through the resonators with an Agilent Technologies N5232A PNA-L vector network analyser (VNA), which has an operating range from 300kHz - 20GHz. To perform this measurement, microwave (MW) signals are sent into the resonator (port 1), and the transmitted signal is measured at the output (port 2). This type of measurement is called an S_{21} transmission measurement (see section 2.1.5), and is typically the chosen method of Q-factor measurement

in CPW resonators [5, 22, 92, 94, 143].

In our experiment, the VNA acts as both the source and detector, which ensures that the input and output signals are phase-locked. In a measurement loop that is not phase-locked, the phase information at the detector is not meaningful, and is unable to be interpreted. Correct phase data is essential, as most fitting algorithms are heavily dependent on the form of the resonance in the complex plane (see figure 2.3) [5, 94]. As seen in equation 2.17, the interpretation of both the environmental and ideal-resonator's contribution to the resonance is dependent on the signal's phase. Typically, the complex S_{21} transmission is broken into a magnitude and phase component (or real and imaginary) for visualisation and data analysis [22].

In this experiment, the VNA was configured to save the transmission data as a `.dat` file containing the frequency of the transmitted microwave, and the real and imaginary components of the S_{21} transmission, as measured by the VNA's detector. These data files were then passed into Probst's [5] circle fit algorithm, which was used to determine Q_i, Q_c, $\langle n_{ph} \rangle$ and the associated uncertainties.

5.3 Measurement circuit

When setting up a measurement circuit for sensitive low-power measurements, such as single-photon S_{21} complex transmission, noise should be minimised, and any un-needed frequencies should be removed through filtering. In other words, the circuit should be designed to maximise signals within the frequency range of the measurement, which is 4 - 8GHz in our case, and minimise signals outside of it. Figure 5.2 shows the measurement circuit components which are inside the Bluefors small dilution refrigerator. In addition to the components inside the fridge, we used in-line attenuators at room temperature to reduce the source power.

In our measurement circuit, an input power of approximately $P_{\text{app}} \approx -141\text{dBm}$ corresponds to an average of 1 photon flux per second; $P_{\text{app}} \approx -141\text{dBm} \rightarrow \langle n_{ph} \rangle \approx 1$. Our VNA microwave source can output signals from -30dBm to 16dBm. In order to reach powers in the range of the single photon limit at least 100dB of additional attenuation is required. As seen in figure 5.2, three XMA 2082-6418-20 CRYO attenuators are placed between the SD fridge's input port and that sample. One at $T \approx 4\text{K}$, another at $T \approx 1\text{K}$, and the last on the fridge's mixing chamber at $T \approx 20\text{mK}$. Each of these attenuators contributes -20dB of attenuation to the microwave signal, resulting in a total of -60dB attenuation inside the SD fridge. We also determined that the signal was further attenuated by approximately -30dB due to the non-zero resistance in cables and circuit components such as filters and circulators. The exact magnitude and sources of the environmental attenuation will be discussed in relation to the measurement of the MAO and LAO resonators in chapters 6.1 and 6.2 respectively.

To minimise the detection of high-frequency noise, we use a K&L Microwave 6L250-12000/T26000-0/0 S/N 184 12KHz low pass filter between the sample output and detector (VNA). Ideally, we would also use a high pass filter at (or below) 4GHz to remove low frequency noise, however we did not have the available hardware to achieve this at the time of measurement. A Low Noise Factory LNF-CICIC4_12A cryogenic dual-junction circulator

with an operating range of 4 - 12GHz was used on the sample's output to minimise signals reflecting back into the resonator. Reflected signals may result in standing waves on the resonator chip's transmission line, which would result in massively deformed resonances that may be unable to be interpreted, as discussed in section 2.1.5.

After the low-power microwave has passed through the resonator, filter, and circulator, the signal is amplified before reaching the detector. To minimise attenuation after the sample, superconducting aluminium cables are used on the output line for all connections on the fridge's mixing chamber, still ($T \approx 1$K), and $T = 4$K stage. We use a Cryo 1-12 SN685 D high-electron-mobility transistor (HEMT) at $T \approx 4$K to amplify the signal by about +30dB. The signal is then passed out of to room temperature, where it is further amplified by a MITEQ AFS3-00101200-42-LN (+27dB gain, operating range of 0.1 - 12GHz) and a Mini-Circuits ZX60-83LN12+ (+21.5dB gain, operating range of 0.5 - 8GHz). All components in the measurement circuit were chosen to allow for maximum throughput of microwave signals in the range of the natural frequencies of our CPW resonators (4 - 8GHz).

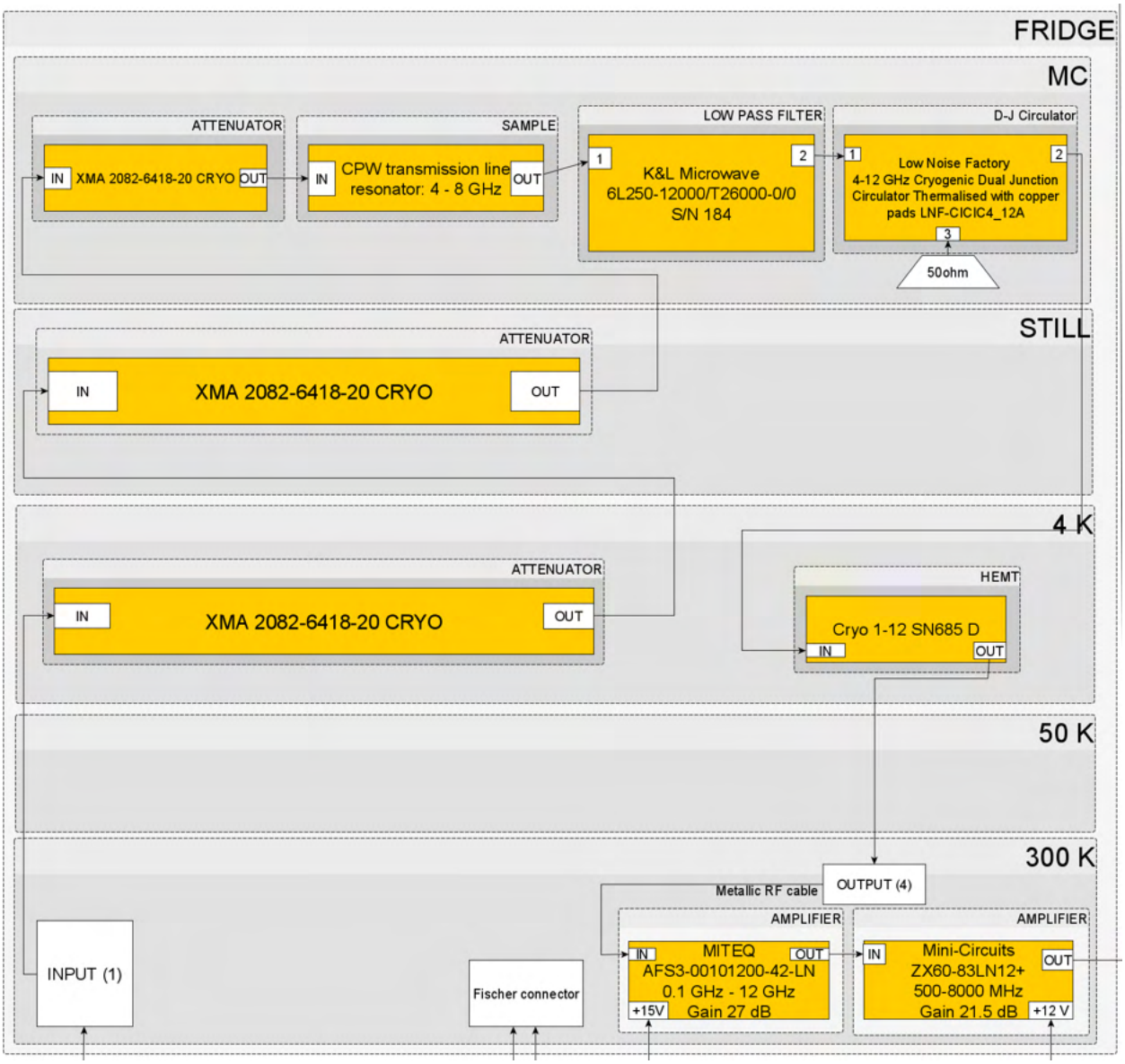


Figure 5.2: Measurement configuration schematic diagram, made using yworks yEd software. The schematic shows all attenuation, filtering and amplification inside the BlueFors small dilution refrigerator. The schematic segments the fridge into different stages at temperatures of 300K (on top of fridge), 50K, 4K, still, and the mixing chamber (MC), which was at a temperature of 29.5mK during measurement. The input line has a total of -60dB attenuation before the sample inside the SD fridge. The output passes through a low pass filter at 12GHz, and a dual junction circulator with an operating frequency range of 4-12GHz. The signal is then amplified by a high-electron-mobility transistor (HEMT) amplifier at 4K, then by two room temperature amplifiers, before being sent to the vector network analyser (VNA). A further -60dB of attenuation was placed between the signal generator and the fridge's input, resulting in a total hardware attenuation of -120dB.

6 Results

Here we discuss the fabrication outcomes and Q-factor measurements of superconducting microwave resonators consisting of a 100nm Al film on either a 1mm thick $MgAl_2O_4(100)$, or 0.5mm thick $LaAlO_3(100)$ substrates obtained directly from MTI Corporation. In both cases, we first reflect on an unsuccessful fabrication attempt, then move to our successful fabrication and operational testing of the final device in SQD Lab's cryostat. The primary source of error in fabrication was found to be in the spin-coating recipe, which resolved fabrication issues for both the MAO and LAO chips. We compare the two devices with each other, and with an equivalent Al on Si CPW resonator chip, used as the *standard material* benchmark.

6.1 $MgAl_2O_4$ devices

The MAO device produced higher internal Q-factors than the LAO and Si devices in both the low and high power regimes. Due to experimental constraints during the measurement of LAO and Si devices, we were able to collect the most data for the MAO device. Here, we discuss the fabrication and operational performance of the MAO device. The highest measured Q_i in the single photon limit was $Q_i = 99000 \pm 7000$ for the 5.9GHz MAO resonator.

6.1.1 Unsuccessful fabrication

Our first fabrication attempt was unsuccessful due to issues associated with lithography. All substrate preperation and film deposition was identical to the methods described in section 4. In this discussion, we compare the unsuccessful fabrication parameters with the successful recipe presented in table 4.1. We did not fabricate this device beyond the etching stage. Figure 6.1 shows optical microscope images of the device after etching, and before resist

removal (i.e. the film surface is still coated with photoresist in areas that aren't etched). There are many visible issues with the lithography on these devices;

- large amounts of photoresist residue remain in the gap (figures 6.1a, 6.1d)
- gap and width dimensions are not consistent with design (figure 6.1b)
- photoresist coating is not even across the chip (figure 6.1c)

Through further recipe testing and optimisation, we found that all of these issues could be causally linked to the spin coating stage of lithography. The exposure, development and etching stages are all highly sensitive to resist thickness.

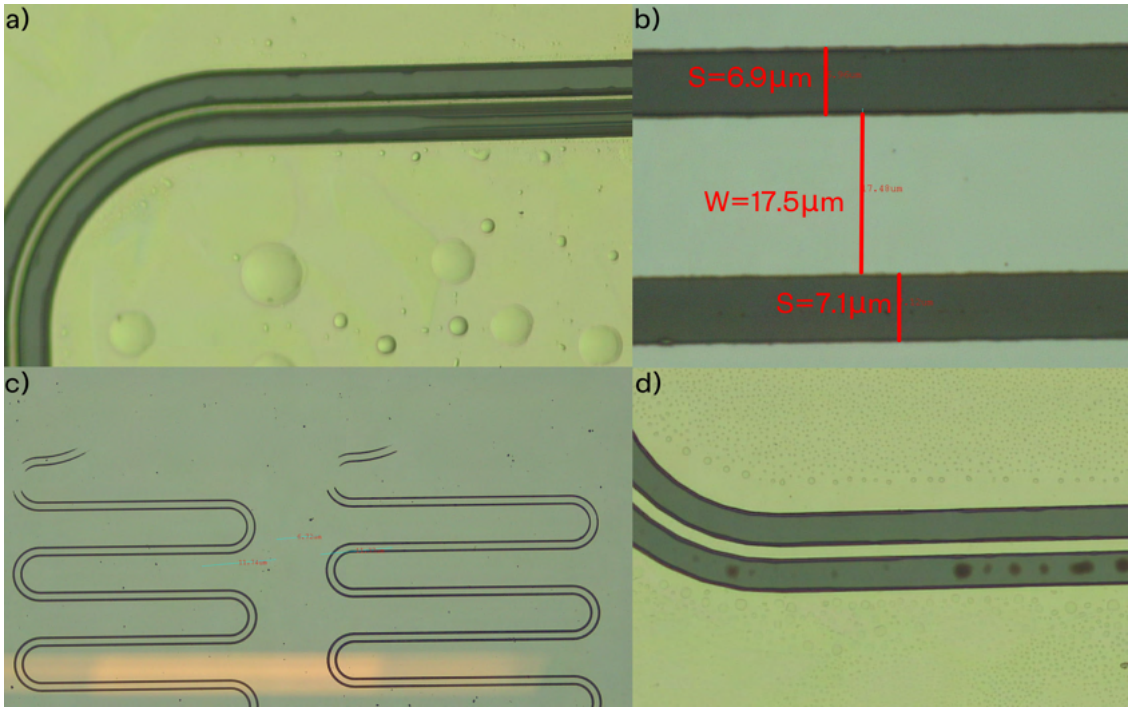


FIGURE 6.1: Optical microscope images of an unsuccessful fabrication attempt using an MAO substrate. The images were taken after etching, and before photoresist removal. Image **a)** shows residual photoresist on the walls of the gap. The measured dimensions of the gap (S) and width (W) are shown in panel **b)**. The intended dimensions are $S = 8$µm and $W = 14$µm. In panel **c)**, we see unexposed areas as a result of the non-uniform thickness of the photoresist layer. Image **d)** shows another example of photoresist residue, this time in the middle of the gap.

These samples were spin coated on the Sawatec SM-200 spin coat module at an 4500RPM for 60s. This is 1300RPM less than the rotation speed of the spin coat recipe used for successful fabrications. The thickness of the photoresist layer was measured with a Dektak 150 surface profiler as 1.6 ± 0.2µm. This is approximately 0.3µm thicker than the optimised recipe. Using the exposure parameters described in section 4.4.2, we found that the device was slightly underexposed, resulting primarily in the walls of the structure not being fully exposed (see figures 6.1a and 6.1d). As we will see in section 6.2, we faced the same issue

with the fabrication of LAO devices using the same spin coating recipe. This residual photoresist is by nature a lossy material, and is in an area of very high field density. There will therefore be a high density of TLS interacting with a high field density. In the single photon regime this scenario would be extremely lossy, and likely translate to very low-Q resonances. Apart from the residual photoresist, underexposure also results in incorrect dimensions of the lithographed structure. As seen in figure 6.1b, the gap (S) is smaller than the intended geometry by approximately 1µm, and the width (W) larger by approximately 3.5µm. This will result in the feedline not being impedance matched to 50Ω, causing a large amount of loss due to reflections at the input and output. In extreme cases, this would result in the device being completely dysfunctional.

Increasing the rotation speed during spin coating also improves the uniformity of the photoresist layer [144]. At the lower rotation speed, we observed highly non-uniform resist thicknesses which, in the worst case, resulted in some sections of the design being completely unexposed as seen at the top of figure 6.1c.

In an attempt to resolve the underexposure, we slightly over-developed the samples. The aim of this was to remove the residual resists that remained on the walls of the structure, and to allow enough time for even the underexposed areas to be developed. Unfortunately, this method produced extremely non-uniform results, and added considerable roughness to the gap walls. Furthermore, this did not resolve the issue of incorrect dimensions, and also did not remove residual resist. Overall, the method was unsuccessful and would have added considerable loss to the device.

To address all of these issues, we progressively increased the rotation speed in the spin coat recipe, and performed the rest of the lithography steps (as presented in table 4.1) until the desired result was produced. The optimal spin coat rotation speed was found to be 5800RPM, which was used for the second round of fabrications for both the MAO and LAO samples.

6.1.2 Successful fabrication

Following the recipe presented in table 4.1, we were able to fabricate high quality Al on MAO microwave resonators. For brevity, the recipe will not be repeated here. Instead, we present and discuss the results of the successfully fabricated resonator chip.

The as-recieved MAO(100) substrate was measured to have a mean roughness of $R_q = 8.0 \pm 0.1$nm. The roughness value was averaged over two measurements from AFM images taken at two different regions on the same sample. After the substrate was annealed and cleaned, the mean roughness was found to have decreased to $R_q = 3.7 \pm 2.7$nm. Unlike the LAO substrate, neither the as-recieved or treated substrates were found to have pronounced terrace structures; AFM images reveal no obvious topographical differences before and after treatment. This likely shows that the surface preperation technique we used is not yet optimised. A well treated MAO surface should exhibit a visible terrace structure similar to LAO [129, 145]. Further improving the substrate treatment process to create a more ordered surface structure could result in higher performance devices.

The deposited Al film was measured to have a thickness of $d = 106 \pm 8$nm with XRR. The plot and fit used to extract d and its uncertainty are shown in figure 6.2a. As mentioned in

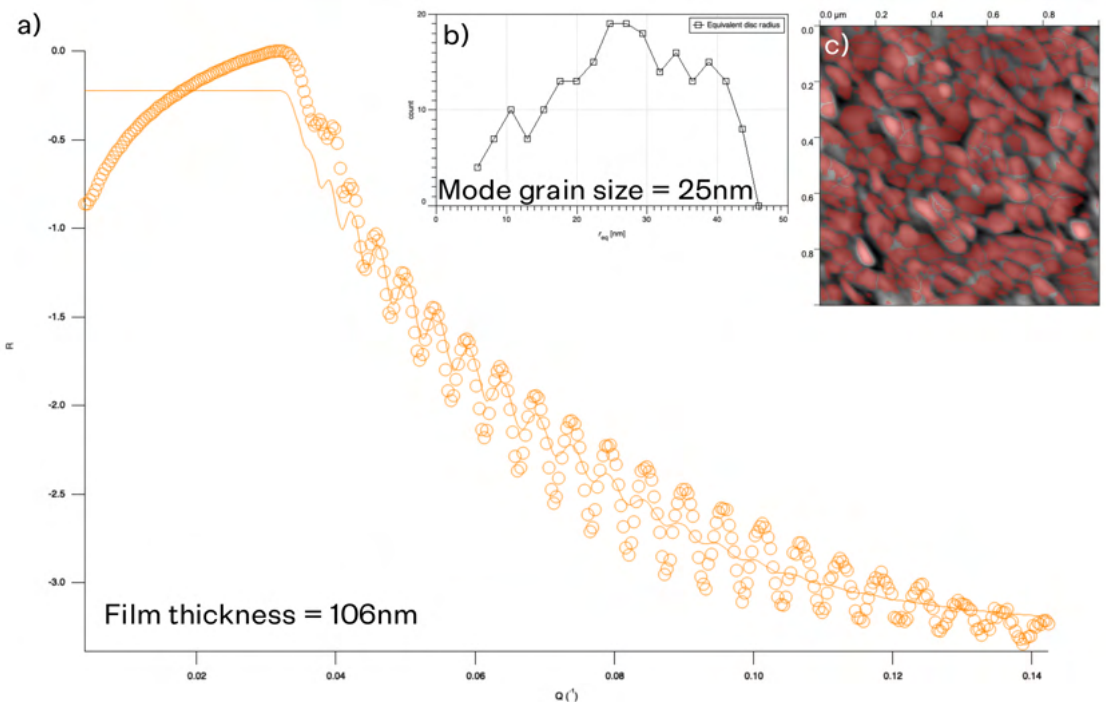
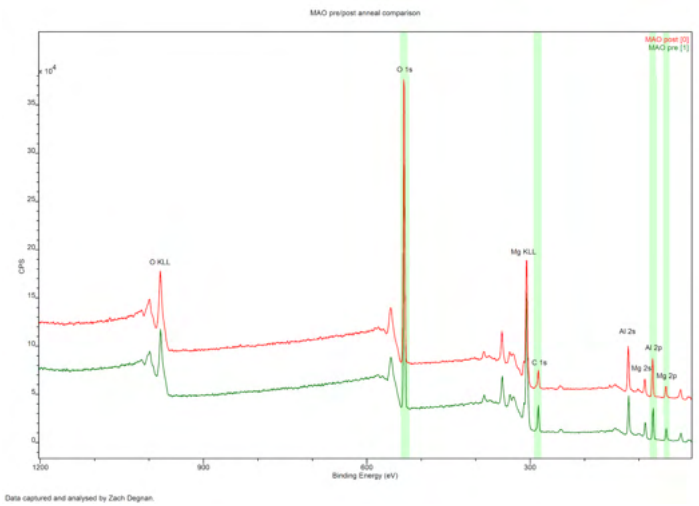


FIGURE 6.2: **a)** Experimental (circles) and fitted (solid line) X-ray reflectivity curves plotted in `Motofit` [20]. The extracted film thickness is $d = 106 \pm 7$nm. Graph **b)** shows the grain size distribution calculated from image **c)**. Grains were marked using Gwyddion's watershed method, and measured by the `statistical quantities` feature in `Gwyddion`. The mode grain size was measured to be 25nm, distributed between 6 - 46nm.

section 3.3, we are only interested in extracting the film thickness from XRR measurements, so our fit is satisfactory as long as the period of oscillations (Kiessig fringes) in the reflectivity signal are replicated by the fit. The Al grains have an equivalent disc radius distributed between 6 - 46nm, with a mode of 25nm. The grain size distribution and the AFM image from which it was calculated is shown in figures 6.2b and 6.2c. The film was measured to have a RMS roughness of $R_q = 4.5 \pm 2.0$, similar to that of the treated MAO substrate.

When characterising the MAO substrate under XPS, we use the characteristic Al 2p, O 1s, Mg 2p and C 1s (contamination) peaks for analysis. XPS results show that the substrate preperation process was successful in decreasing carbon-based surface contamination by approximately 5%. The relative ratio of Mg:Al:O (ideally 1:2:4 for $MgAl_2O_4$) was measured as 1.0:1.8:3.2 before treatment and 1.0:2.0:3.6 after treatment (neglecting carbon contamination). The high resolution scans of each peak before and after surface treatment are shown in appendix A.2.

The etched structures displayed besides the intended geometries are shown in figure 6.4. Using optical microscopy, the lithographed geometries were measured to be within $\pm 0.5\mu$m of the intended geometries. No residual photoresist could be seen by optical microscopy. After lithography, the wafer was successfully diced into the 14 individual circuits. One circuit was then chosen to setup for measurement.



Pre-anneal atomic concentration

Name	Position	FWHM	Raw Area	%At Conc
Al 2p	74.00	2.81	95889.8	24.18
C 1s	285.00	2.90	86900.6	18.73
O 1s	531.00	3.07	814223	43.63
Mg 2p	50.00	2.77	34868.1	13.46

Post-anneal atomic concentration

Name	Position	FWHM	Raw Area	%At Conc
Al 2p	75.00	2.81	114239	26.60
C 1s	285.00	2.99	65600.5	13.05
O 1s	532.00	3.01	954103	47.19
Mg 2p	50.00	2.88	36938.4	13.16

FIGURE 6.3: XPS survey scans before and after substrate preperation, plotted and analysed with CasaXPS. The two plots are vertically offset for viewing purposes. The atomic concentrations corresponding to each survey scan are listed, as calculated from the characteristic XPS peaks for MAO. We see that the surface density of O and Mg increase after substrate preperation, and a considerable amount of carbon-based contamination is removed by annealing.

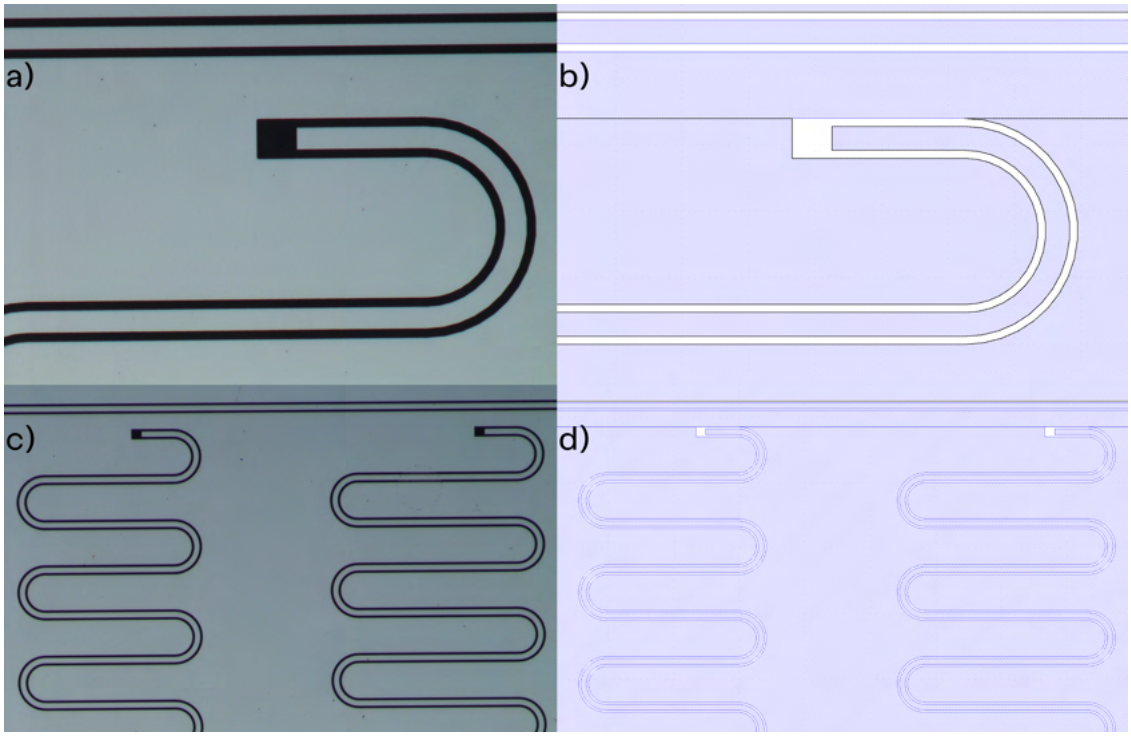


FIGURE 6.4: Optical microscope images of a successful fabrication on an MAO substrate. The images are displayed next to the intended designs taken from `klayout`. The microscope images were taken after etching and photoresist removal. Images **a)** and **b)** show the lithographed and digital design of a coupling region respectively. Panels **c)** and **d)** compare the lithography and design of two $\lambda/4$ resonators.

6.1.3 Device measurement

The device imaged in figure 6.4 was setup for measurement in the cryostat according to the procedure detailed in section 5. The measurement setup was completed with help from Eric He, Rohit Navarathna and Alejandro Gomez Frieiro of SQD Lab. All measurements took place over a period of 12 hours, whilst the cryostat's mixing chamber was kept at a stable temperature of 29mK. The extracted high and low power Q-factors (Q_H and Q_L respectively), and their associated uncertainties are given in table 6.1. The full range of powers measured on the MAO chip ranged from $\langle n_{ph} \rangle \approx 10^{-1}$ to $\langle n_{ph} \rangle \approx 10^4$, corresponding to input powers of -150dBm and -104dBm respectively. The S_{21} transmission was measured and Q-factors were fit at 1dBm increments across the power range. We measured each resonator individually by selecting a small sweep range of width 1.2MHz around the resonance frequencies listed in table 6.1. The Q_i power dependence for each resonator is plotted in figure 6.5. Various scripts used for measurement (VNA control), fitting, and plotting can be found in appendix A.3, where we have also included some example high and low power Q-factor fits. To the best of our knowledge, these are the highest Q_i superconducting resonators fabricated on MAO substrates to date.

Frequency [GHz]	$Q_L \times 10^4$	$Q_H \times 10^4$
4.806	7.7 ± 0.7	48.2 ± 2.5
5.314	8.6 ± 0.6	64.7 ± 1.4
5.969	9.9 ± 0.7	70.9 ± 5.5
6.841	9.1 ± 0.7	48.9 ± 0.7
7.984	9.4 ± 0.7	29.3 ± 0.2

TABLE 6.1: Internal Q-factor (Q_i) measurements of the MAO device. All measurements were performed whilst the cryostat mixing chamber was at $T = 29$mK. Q_H corresponds to a high power measurement with $\langle n_{ph} \rangle \approx 2000$ and Q_L corresponds to a measurement in the single photon regime ($\langle n_{ph} \rangle \approx 1$). Q-factors and their corresponding uncertainties were extracted from S_{21} measurements using Probst's circle fit algorithm [5], available from GitHub [23]. Examples scripts that were used to perform the measurement and fitting procedures are included in appendix A.3.

The photon number was calculated according to equation 2.16, which is implemented in Probst's circle fit algorithm [5]. The calculation of average photon number flux per second in the resonator cavity requires knowledge of the absolute power going into the resonator chip's feedline. We have good knowledge of the source attenuation (controlled by VNA), and the manual attenuation inside and outside the fridge, however we do not know the exact environmental attenuation of the signal from source to the chip's input. This additional power loss could come from cable attenuation, and losses at the chip bonds (on input or output). Calibration testing was done to approximate the additional environmental attenuation. As we were unable to make a measurement to test the exact location of each bit of additional attenuation, we assume that -20dBm is attenuated between the source and the sample, and the remainder of attenuation occurs after the sample. We therefore approximate the additional -20dBm of attenuation on the source. We were able to measure that the source cables contribute -10dBm of attenuation, so it was concluded that the additional -10dBm

was most likely lost due to attenuation as the signal passes through the wire bonds from the PCB to the chip's transmission line.

As seen in figure 6.5, Q_i decreases at lower powers for all five resonators. As discussed in section 2.1.5, this is due to the fact that TLS become unsaturated in the lower power regime, leading to a higher loss ratio [46]. From this result, we can conclude that there are still a significant amount of TLS present in our devices. The highest performing resonator at both $\langle n_{ph} \rangle \approx 2000$ and $\langle n_{ph} \rangle \approx 1$ was the resonator at $f_0 = 5.97$GHz. All resonators had similar performance and power dependence, as shown in figure 6.5. This indicates that none of the resonators were damaged during fabrication. In section 6.3, we discuss methods that could further decrease TLS losses.

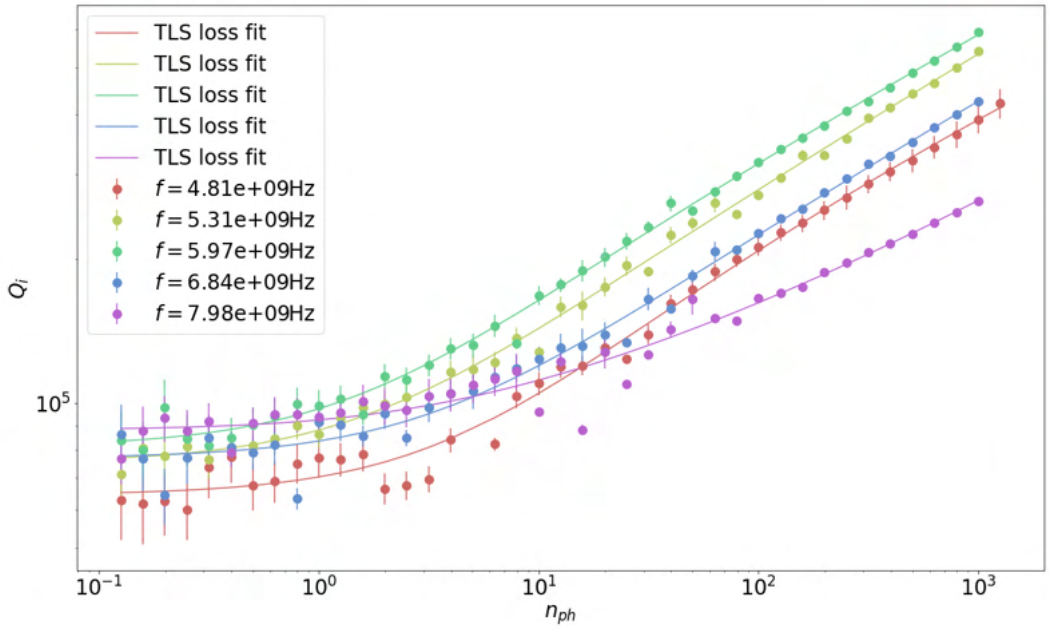


FIGURE 6.5: Q_i power dependence of all five resonators on the MAO chip. The minimum input power corresponds to -150dBm, and the maximum to -104dBm. The TLS loss model presented in equation 2.18 was used to fit the power dependence. The script used for fitting and plotting can be found in appendix A.3.

6.2 $LaAlO_3$ devices

Here we present fabrication and performance results for the LAO devices. The internal Q-factor was found to be lower than the MAO chip and higher than an equivalent Al on Si chip. The highest measured Q_i in the single photon limit was $Q_i = 99000 \pm 7000$ for the 5.9GHz MAO resonator. Due to constraints on VNA usage, we were only able to measure the power dependence of Q_i on one LAO resonator.

6.2.1 Unsuccessful fabrication

During our first attempt at fabrication on LAO, we faced issues very similar to that of the unsuccessful MAO fabrication described in section 6.1.1. We found, however, that the results of underexposure were more pronounced in certain areas on the LAO samples. This is likely due to the twin domain crystal structure of LAO [146] causing non-uniform photoresist thickness across the sample. Optical microscope images of the failed LAO fabrication at various stages in the procedure are shown in figure 6.6.

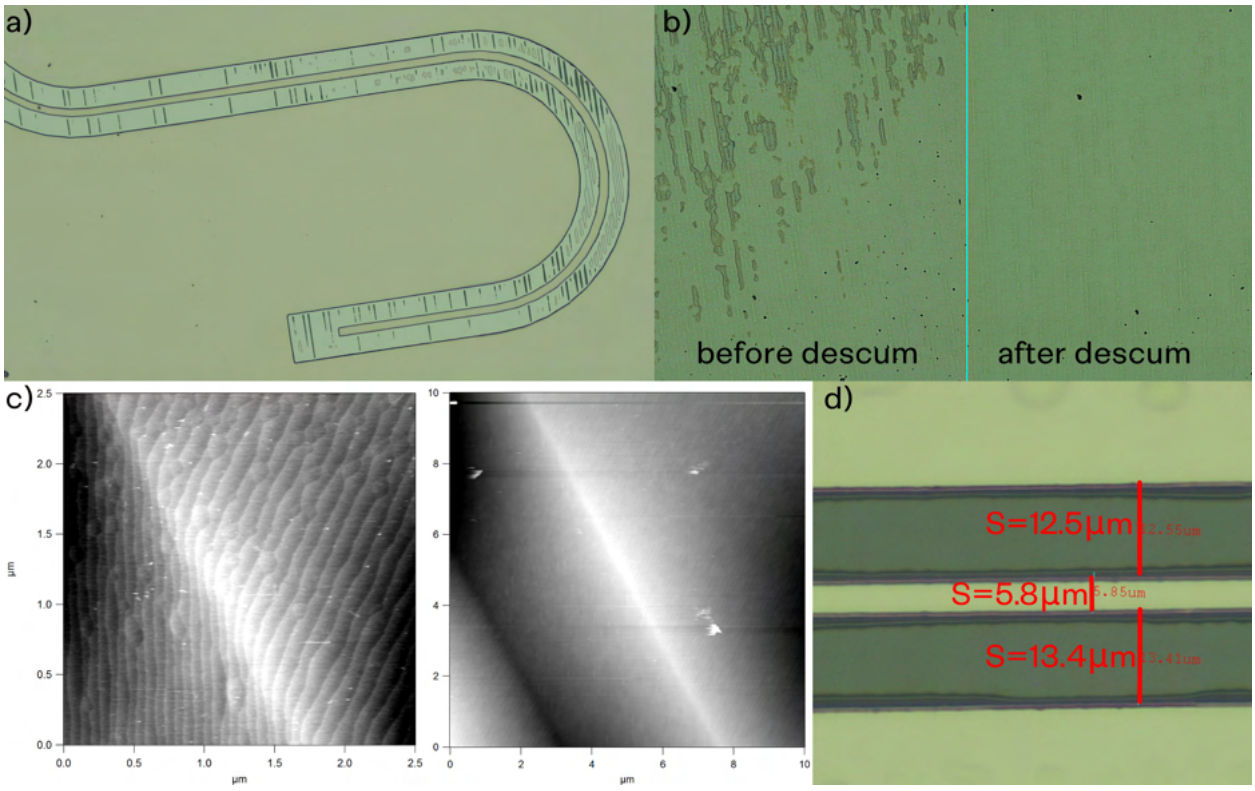


FIGURE 6.6: **a)** Lines of residual photoresist (black lines visible in gap) left after development due to underexposure. **b)** Residual photoresist on a particular contact pad before and after an O_2 descum. The images shown that the descum process was successful in removing the residue, which is seen as the darker streaks. **c)** AFM height images of twin domain boundaries in LAO, showing the saw-wave like peaks at the boundaries. The left image is 2.5 × 2.5µm, and the right image is 10 × 10µm. **d)** Measured dimensions of lithographed structure after etching. The dimensions are within 0.5µm of the intended design, however a large amount of residual photoresist (seen as the darker grey colour lining the walls) remains in the gaps.

The twin domain structure is induced when the sample is cooled through the phase transition at $T_c = 544°C$ [146] during the annealing stage of our substrate preperation. As shown in figure 6.6c, the domain boundaries are peaked structures. If one were to take a line profile across multiple domain boundaries, it would have a saw-wave structure. This adds considerable roughness to the substrate surface, leading to less evenly dispensed photoresist. Areas that were heavily underexposed, such as the area pictured in figure 6.6a, were likely

in the *valleys* of the crystal structure, meaning that the resist layer would have been thicker here.

In an attempt to remove the lines of residual photoresist from the developed areas, we performed an O_2 descum clean in an Oxford Instruments PlasmaPro NGP80 reactive ion etcher (RIE) located at ANFF-Q. O_2 descum is a low-temperature technique, in which a sample is etched with O_2-plasma to remove organic residuals. It was found that the 60s descum did not change the structure geometry, but was successful in removing a significant amount of residual photoresist, as shown in figure 6.6b. In future fabrications, we recommend the use of an O_2 descum after development in order to remove residuals that may not be visible by optical microscopy.

Similar to MAO, the gap and width dimensions (see figure 6.6d) did not agree with the intended design. Using the initial spin coating recipe (1.3µm photoresist layer), the lithographic process resulted in over etching by approximately 1µm). Furthermore, a large amount of residual photoresist was found in the gap. This shows us that the descum process, whilst successful in removing small amounts of resist residues, was not consistently effective at removing all resist from edges. This indicates that a longer descum treatment would be needed, however intense O_2-plasma cleans have been shown to degrade Q_i [101]. A more gentle method of photoresist residue removal, such a supercritical CO_2 drying [112], may be more useful.

6.2.2 Successful fabrication

18 individual circuits were fabricated on an LAO substrate according to the recipe given in table 4.1. The as-recieved LAO(100) substrate was measured to have an RMS roughness of $R_q = 1.6 \pm 0.2$nm by AFM analysis. The surface roughness was found to increase dramatically after annealing to $R_q = 2.5 \pm 1.3$nm and then decrease again after DI water leaching to a final roughness of $R_q = 0.9 \pm 0.2$nm. As seen in figure 6.7, the surface order also improved dramatically over the treatment process. The roughnesses were determined by AFM image analysis in `Gwyddion`, and the uncertainties were estimated as the standard deviation of multiple roughness values measured at different regions on the same sample. Figure 6.7e shows the surface's step profile after treatment. The steps have a height of 3.6 ± 0.4Å, corresponding to lattice constant of LAO. From this, we can deduce that the surface has been ordered into an atomically accurate step structure.

The effect of DI water leaching is obviously a very important step in producing a uniform surface. We characterised the surface with XPS before and after DI leaching, and found that a considerable amount of La is removed from the surface by the process. Kim et. al [108] found that a La_4O_5 surface reconstruction can occur during high temperature annealing, causing mixed surface termination. From the AFM phase images seen in figure 6.8, we were able to identify two primary surface components. Comparing AFM data with XPS results, we were able to identify one of the components as islands containing La. The highlighted regions in figures 6.8a and 6.8b are likely islands of La_4O_5 molecules, whilst the rest of the surface is AlO_2 terminated. The concentration of the La islands were found to decrease after DI water leaching, consistent with our XPS results and the results of Kim et. al [108]. XPS results revealed that the La surface component decreased by 15.9% after DI leaching, and

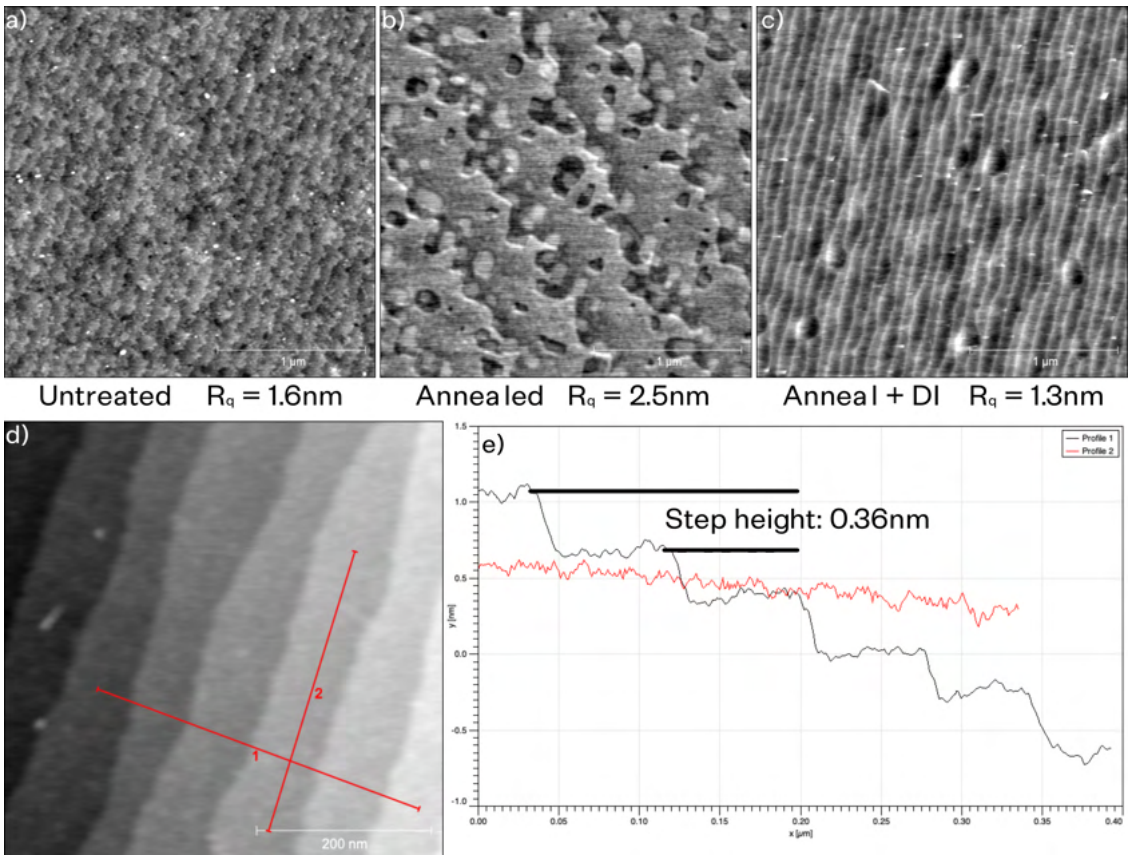


FIGURE 6.7: 2.5µm AFM images of the LAO substrate **a)** before, **b)** during (after annealing, but before DI water leaching), and **c)** after surface treatment. Note that images a) and c) are taken on the same sample, but image b) was taken on a separate sample, hence the different terrace width. Panel **d)** shows a 0.5µm AFM image of the terrace structure on the treated substrate. The line profiles along (1) and (2) are shown in panel **e)**. The profile running down the steps (1) is shown in black, whilst the profile running along a single step is shown in red. The step height was measured to be 3.6 ± 0.4Å. All AFM images were taken on the Asylum Instruments Cypher AFM located at ANFF-Q. An Etalon HA_FM AFM tip was used.

AFM analysis gives a 15.8% decrease, as shown in figure 6.8. These two results agree well. Kim et. al found that the LaO surface component is gradually dissolved in water, explaining the removal of LaO islands by DI leaching [108].

Neglecting the presence of carbon (or any other elements), the atomic concentrations of the as-recieved LAO surface were found to have an La:Al:O ratio of 1.0:1.2:3.6 (ideally 1:1:3). This result shows that the as-recieved surface is oxygen deficient. After annealing, the surface oxygen component was reduced slightly further to 1.0:1.2:3.5. Finally, after DI water leaching our surface atomic concentrations yield a ratio of 1.0:1.6:4.5. Relative to the ratios after annealing, we can see that the Al and O components increase relative to the La component. This corresponds to a 15.9% decrease in the La component. As seen in figures 6.8c and 6.8d, high resolution XPS scans of the La 3d doublet peak also reveal a change in the chemical structure of the La component after DI leaching. This is likely due to the La

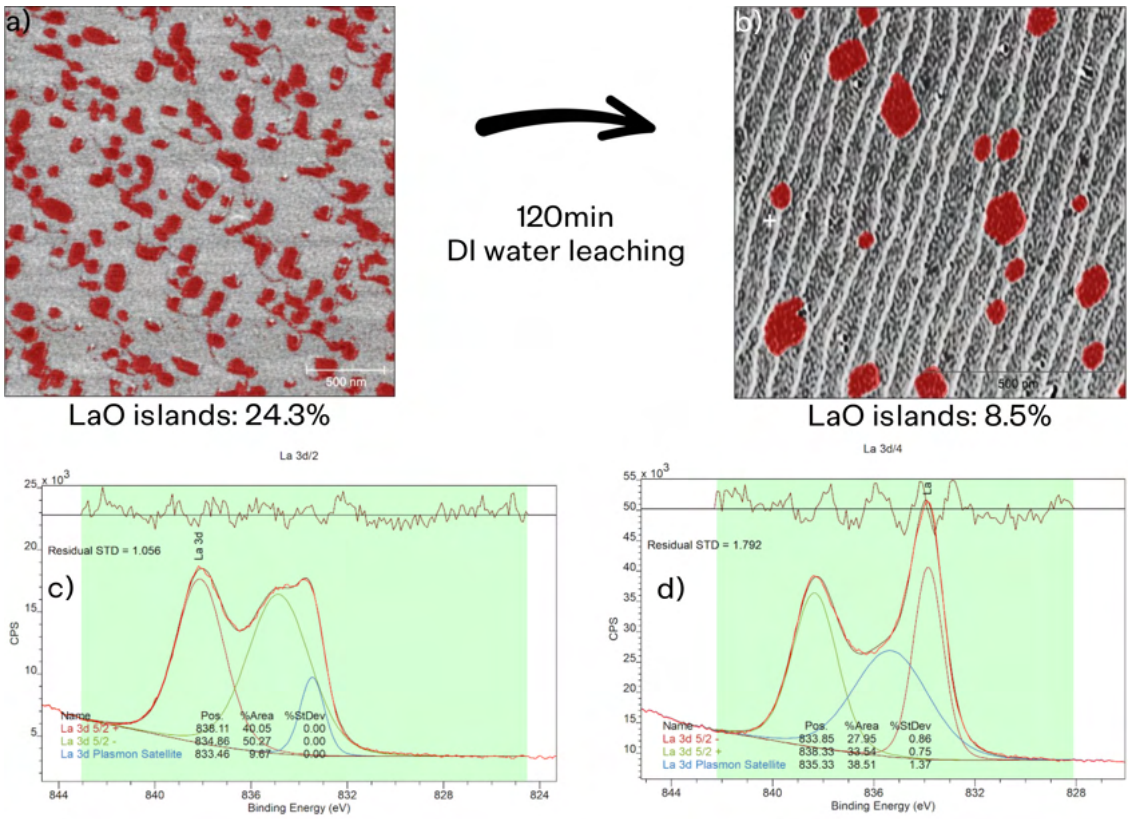


FIGURE 6.8: Panel **a)** shows an AFM phase image of the LAO substrate after a 1200°C 3hr anneal, and before DI water leaching. Regions with different mechanical properties (detected by the phase channel of tapping mode AFM) are highlighted in red. These same regions are again highlighted in panel **b)** on an AFM phase image taken after DI water leaching. The region concentration decreased from 24.3% to 8.5%, and the remaining islands coalesced to form slightly bigger islands. Panels **c)** and **d)** show the change in the La 3d doublet peak before and after DI leaching, as captured by XPS. The peak changes form, corresponding to a change in the chemical bond structure of La on the surface. XPS data visualised and analysed with `CasaXPS`, and AFM data analysed with `Gwyddion`.

being primarily bound as La_4O_5 before DI leaching, and LaO after.

XPS characterisation also revealed that carbon was reintroduced to the surface by the process. This could either be due to contamination during transport from the UQ Long Pocket campus where annealing was done, to the St. Lucia campus where the DI water leaching was done, or unclean beakers or DI water in which the leaching was done. The contamination was more likely to arise from transport, as the DI water (with a resistivity of 18.2MΩ cm) was collected from a Milli-Q dispenser directly before leaching, and the borosilicate glass beaker used for leaching was thoroughly cleaned with VLSI IPA. In future, a more suitable device transportation vessel (such as a portable vacuum desiccator) should be used to minimise contamination between fabrication steps.

The Al film was characterised with AFM and XRR, as shown in figure 6.9. We confirmed the nominal film thickness of $d = 100 \pm 5$nm fitting our XRR data for the film thickness

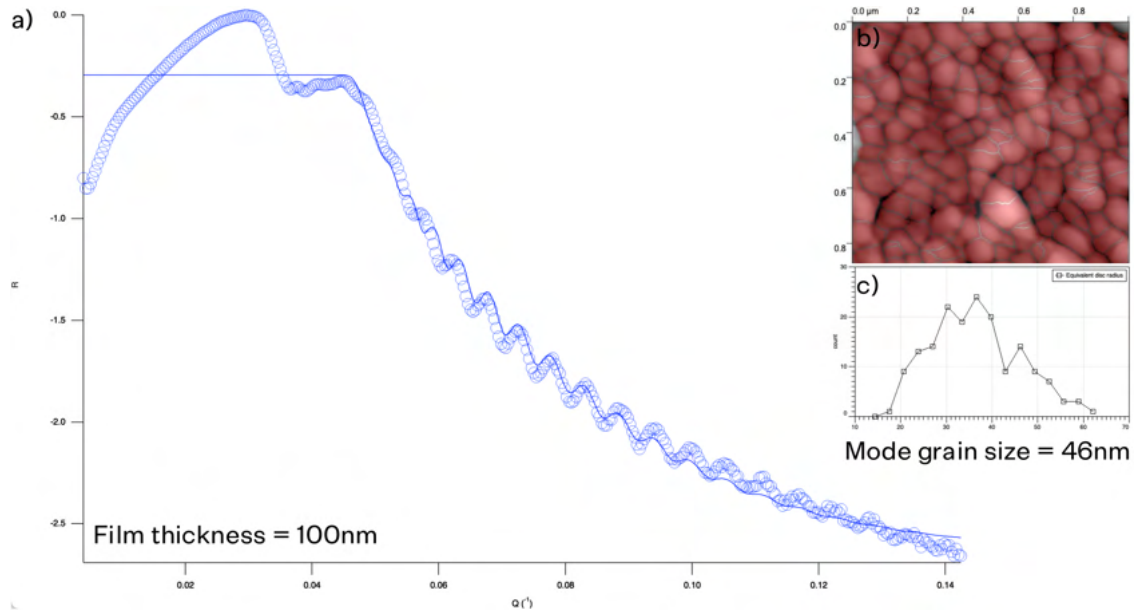


FIGURE 6.9: **a)** Experimental (circles) and fitted (solid line) X-ray reflectivity curves plotted in `Motofit` [20]. The extracted film thickness is $d = 100 \pm 5$nm. Graph **c)** shows the grain size distribution calculated from image **b)**. The mode grain size was measured to be 46nm, distributed between 15 - 63nm.

parameter. The grain distribution was found to be more uniform in shape and distribution on the surface than those grown on the MAO substrate. The mode grain size calculated as 46nm, with a distribution from 15 - 63nm. The mode grain size for Al grown on LAO was over 20nm larger than those grown on MAO. Using AFM analysis, the roughness of the film surface was measured to be $R_q = 2.0 \pm 0.3$nm. It is hypothesised that grain boundaries could host a high density of TLS, so having larger grains could in theory reduce TLS losses on the MA interface. The LAO chip has a smaller conductor width than the MAO chip, so the field density at the conductor's surface (MA interface) will be greater [46].

Figure 6.6 shows the result of lithography on the LAO chip. The gap and width dimensions were measured with an optical microscope, revealing that the gap was over etched by approximately 0.5µm during lithography. This is likely due to either the development or etching time being slightly too long. These parameters should be further optimised for future fabrications to ensure the device is impedance matched and coupled as intended. From the asymmetric line shape of the measured resonances on the LAO chip, it is clear that the transmission line is not well impedance matched, which is likely due to the small change in dimensions. A decreased gap/width ratio (as in the case of over etching) will result in a larger transmission line impedance [15, 87].

6.2.3 Device measurement

The LAO device was measured in the same conditions as the MAO resonators (see section 6.1.3). However, in the case of LAO, one of the output cables on the 4K stage of the cryostat was *not* an Al superconducting cable. This means that the LAO measurements

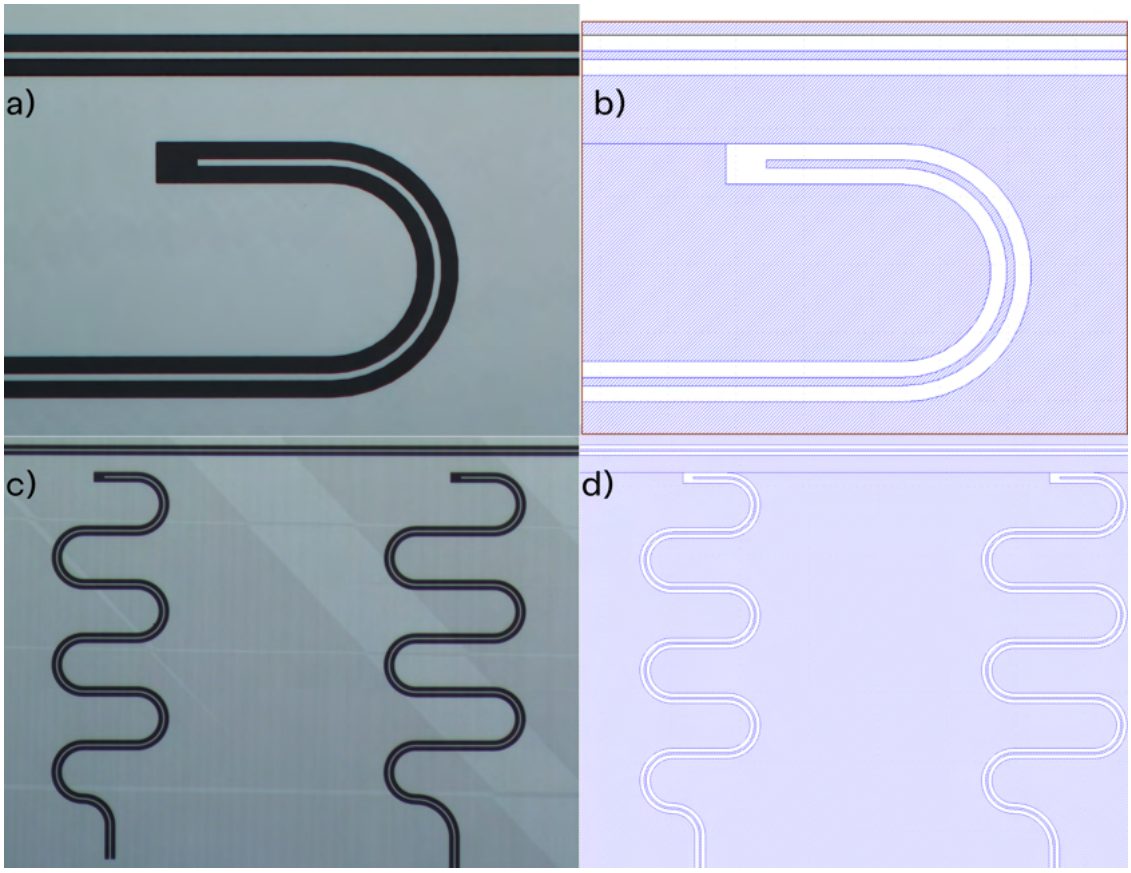


FIGURE 6.10: Images **a)** and **b)** show an optical microscope image of the lithographed design after etching, and a `klayout` screenshot of the intended design respectively. Here, a coupling section is shown. Images **c)** and **d)** show two resonators as lithographed and designed. The diagonal stripes seen in c) are due to the twinned crystal domain structure of LAO (see figure 6.6c).

have slightly more attenuation on the output, leading to a slightly lower signal to noise ratio by the time the signal reaches the VNA. As a result, the low power measurements of the LAO device required higher averaging, and a smaller bandwidth, leading to longer data collection times. The LAO device was measured first, so the 4K output cable was replaced with a superconducting cable for MAO measurements to circumvent this issue. We found that a measurement at the same power took approximately 10 times as long for the LAO chip (approximately 90 minutes for a single photon measurement). All Q-factors and uncertainties were calculated according to the method use for MAO, which can be seen in appendix A.3.

The measured Q-factors for the LAO resonators are shown in table 6.2. We found that the internal Q-factor is underestimated by the circle fit algorithm [5] when the signal is noisier. This was verified by taking measurements at the same power with increased averaging to reduce noise. The Q-factor improved by up to 50% with an improved signal to noise ratio. This result suggests that the low-power Q_i quoted in table 6.2 could be underestimated. We were unable to measure a resonance on the $f_0 = 5.413$GHz resonator with less than approximately 1×10^6 photons in the cavity, far beyond the operational limit. We therefore

have not included this resonator in the results. It is likely that this resonator did not perform well due to contamination in the gap causing excessive losses.

Frequency [GHz]	$Q_H \times 10^4$	$Q_M \times 10^4$	$Q_L \times 10^4$
4.886	25.5 ± 4.9	7.4 ± 0.5	5.9 ± 1.1
6.066	*NM*	*NM*	3.8 ± 0.3
6.895	*NM*	7.9 ± 0.4	*NM*
7.995	14.3 ± 0.5	7.7 ± 0.5	4.6 ± 0.8

TABLE 6.2: Internal Q-factor (Q_i) measurements of the LAO device. All measurement and fitting was as described in table 6.1. Here $Q_M \times 10^4$ refers to a medium power measurement, with $\langle n_{ph} \rangle \approx 100$. We include this category in the table because the low power resonances could not be successfully fit for certain resonators due to the low signal to noise ratio. We were unable to measure a resonance on the 5.413GHz resonator. *NM* stands for *not measured*.

Figure 6.11 shows the dependence of Q_i on power for the resonator at $f_0 = 4.886$GHz. As observed on the MAO chip, we see a decrease in Q_i with decreasing input power due to TLS losses. The measured Q-factors at lower powers ($\langle n_{ph} \rangle < 10^1$) have relatively large uncertainty due to the amount of noise present in the signal. It can be seen that measurements at very similar power do not have overlapping error bars, which indicates that the fit model may slightly underestimate errors for noisy measurements.

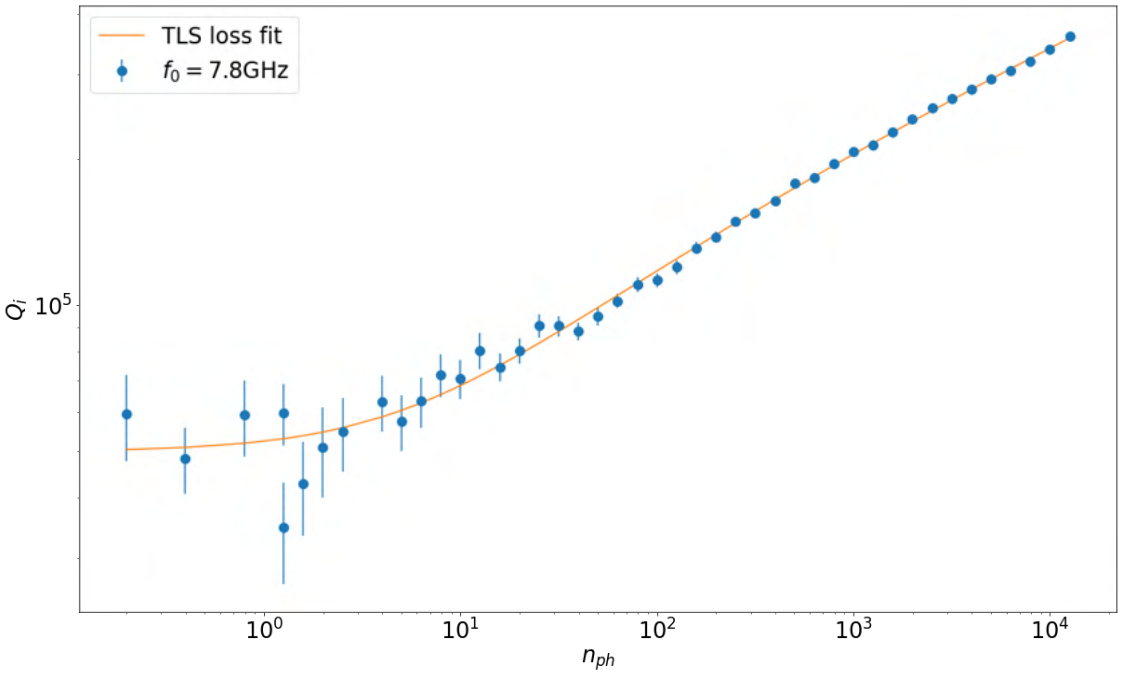


FIGURE 6.11: Q_i power dependence of the 7.8GHz resonator on the LAO chip. The minimum input power corresponds to -146dBm, and the maximum to -101dBm. The TLS loss model presented in equation 2.18 was used to fit the power dependence. The script used for fitting and plotting can be found in appendix A.3.

6.3 Device comparison

Comparing the performance of superconducting resonators can be difficult. In any one device, there are a large number of factors contributing to device performance, including (but not limited to) geometry, material, fabrication processes, measurement setup and data analysis method [22]. Here, we compare the LAO and MAO devices with each other, and with an Al on Si chip. The Si chip was fabricated by Eric He of SQD Lab using the same fabrication processes and instrumentation, and was measured in the same conditions. The geometry and circuit design was also kept constant except for the small adjustments that were required due to the dielectric constant. Here we compare the measured Q_i of the three chips, and discuss differences between the chips and how they may effect the internal quality factor.

Due to experimental constraints, we were only able to measure the Si chip at $\langle n_{ph} \rangle \approx 100$. At this input power, the MAO chip has $Q_i = 31.8 \times 10^4$, LAO $Q_i = 12.0 \times 10^4$ and Si $Q_i \approx 3 \times 10^4$; both the LAO and MAO chips outperform the Si chip. Whilst we cannot conclusively say that both materials are better than Si for low loss superconducting applications, the result is nonetheless promising for the application of LAO and MAO as substrate materials.

As seen in tables 6.1 and 6.2, the MAO device outperforms LAO at *all* input powers. Due to the difference in the dielectric constant of the two materials, the gap/width ratio is much larger for LAO (i.e. MAO has a larger central conductor width than LAO). Therefore, for the same cavity power, there will be a higher field concentration in the central conductor of the LAO chip [46, 53, 113]. This means that any TLS hosted on the metal-air (MA) interface will be more strongly interacting in the LAO sample. The LAO chip has much larger gaps than the MAO chip, so the area of the substrate-air (SA) interface is much larger. Considering these geometries, our results could indicate that the MA and SA interfaces are more lossy than the substrate-metal (SM) interface. This may be due to the fact that these two interfaces are coated with photoresist throughout the fabrication process. If the photoresist was not completely removed, there would still be lossy residues present on both the MA and SA interfaces (but not the SM interface). We aim to test this theory in future studies by applying more rigorous photoresist removal techniques and comparing the results with those measured in this study.

To minimise these losses in general, a future design consideration for CPW resonators would be to minimise the field density at the MA interface by making it wider, and to minimise the area of the SA interface (i.e. maximise the gap/width ratio). Generally, this will be more achievable for materials with lower dielectric constants, as the gap/width ratio increases as the dielectric constant decreases for impedance matched devices [15, 87].

As we saw in section 6.1, the SM and MA interfaces are rougher on the MAO chip. Since we measure higher Q_i on the MAO chip, we could conclude that surface and interface roughness does not have a large impact on device performance. This conclusion was also made by Quintana et. al in their 2014 study of superconducting resonator losses [147]. Another difference between the two chips is in the lattice matching between substrate and film. As discussed earlier, MAO is a better lattice match to Al, which will lead to fewer defects in the deposited film. This could be another reason for MAO's increased Q-factor.

Finally, it could also be possible that the crystal domain boundaries in LAO cause additional losses. We could test this directly by fabricating two LAO chips, one of which was annealed (with the twin domain boundaries), and other with surface treatment that does not require heating the material above the twin phase transition.

Possible fabrication improvements

As discussed in section 6.3, it is likely that a large proportion of our TLS losses arise from TLS hosted in photoresist residue that is left behind after lithography and dicing [22, 30, 147]. In our fabrications, photoresist was removed by cleaning with acetone and IPA. Supercritical CO_2 could be used to perform a post-fabrication clean that would non-destructively remove photoresist residues [112]. We hope to perform a CO_2 clean on one of the remaining MAO circuits, and compare its performance with the solvent-cleaned chip tested on in this study. Another post-fabrication cleaning method is buffered oxide etching, which generally etches the substrate at a much faster rate than the metal film [30]. The exact rates are dependent on the material choice of substrate and film. This technique allows for the complete removal of photoresist and other disordered components from the SA interface without extensively damaging the lithographed structure. This technique was used by Altoe et. al to obtain record single-photon Q-factors in their resonators [30].

Another fabrication technique that has been shown to increase resonator Q-factor is trenching [48, 54, 96]. Trenching refers to further removal of the dielectric substrate in the gap region by etching, so that the SA surface is below the SM interface. The trench depth can range from 1 - 100µm [22, 48, 54], and is commonly done with a dry etching technique such as reactive ion etching (RIE). The idea behind trenching is to decrease the field density at the potentially lossy SA interface. By relocating the SA interface to be far below the SM interface (where the field density is highest), any TLS on the SA interface will not be as strongly interacting, and therefore will have a decreased contribution to losses.

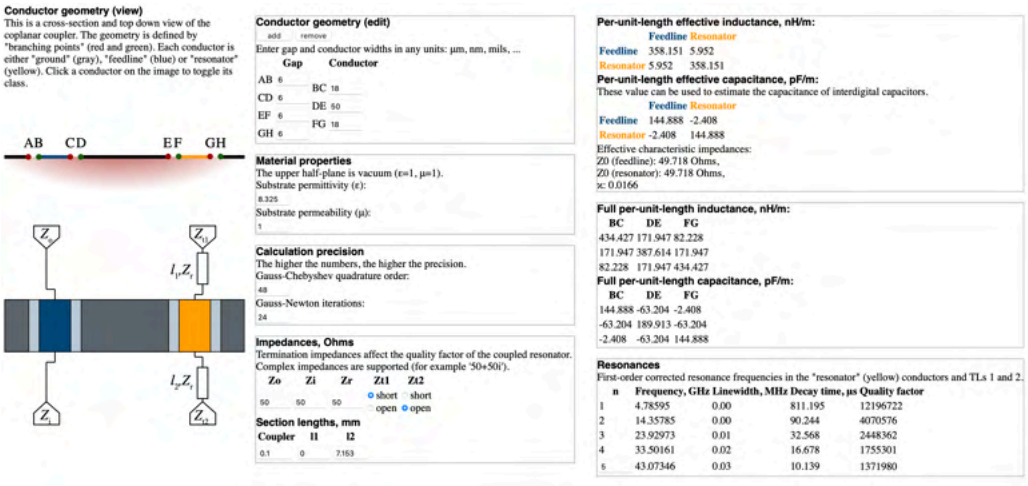
7
Conclusion

In this study we fabricated, characterised and measured the internal Q-factor of superconducting CPW microwave resonators in the quantum regime. Our resonators were fabricated on low-loss dielectric substrate materials, MAO and LAO. Among other reasons, these materials were chosen due to their potential to reduce the device's losses due to TLS interactions. We made two equivalent devices on the substrates, each with a superconducting Al film. We found that the MAO chip outperformed the LAO chip both in the quantum regime, and in the high power regime. In the single photon regime, the best resonator on the MAO chip was measured to have $Q_i = 9.9 \times 10^4$, whilst the best performing LAO resonator yielded a value of $Q_i = 5.9 \times 10^4$. These two devices were also compared with a standard Al on Si resonator which was fabricated and measured under the same conditions as the MAO and LAO chips. At input power of $\langle n_{ph} \rangle \approx 100$, the MAO and LAO chips were measured to have Q_is approximately 10 and 4 times that of the Si chip respectively. To determine exactly where losses are introduced during fabrication, further testing is required. This would involve fabricating and testing multiple devices with varied processes to aid in determining losses added by each fabrication step [111]. We believe that the Q-factors could be further improved to a world-class standard by employing advanced fabrication methods such as substrate trenching [48, 54, 96] and post-fabrication cleaning with supercritical CO_2 [112] or post-fabrication buffered oxide etching [30].

A Appendix

A.1 Python code used to design MAO chip in `klayout`

The following pages show the python code (written and run in a Jupyter notebook), that was used to design the MAO chip in `klayout`. The code makes use of the python package developed by members of SQD Lab. The Klayout-python package is available via Github.



[1]:
```
import klayout.db as db
import os
import numpy as np

working_path = os.getcwd()

# define filename, ClassLib path (path) and path for file save (printpath,␣
 ↪filename)
filename = r'MAOresonator_210303.gds'
printpath = r'/Users/Silk-D/Documents/Klayout-python-master/MyResonatorOutputs'
path = r'/Users/Silk-D/Documents/'

os.chdir(path)
from classLib import *

# Change back to original working directory
os.chdir(working_path)
print(working_path)

# Create a Klayout Layout object
layout = db.Layout()

# Make all numeric references to be in nm
layout.dbu = 0.001
```

```
/Users/Silk-D/Documents/KLayout-python-master
```

1.1 Clear canvas, create a chip and layers

[2]:
```
layout.clear()
cell = layout.create_cell("BasicCell")

class CHIP:

    '''SET INDIVIDUAL CHIP SIZE'''
    dx = 7.1e6 # Chip width in x
    dy = 2.1e6 # Chip width in y

    L1 = 2.5e6
    gap = 18.e3
    width = 6.e3
    b = 2*gap + width
    origin = db.DPoint(0, 0)
    box = db.DBox(origin, origin + db.DPoint(dx,dy))
    # only 4 connections programmed by now
    connections = [box.p1 + db.DPoint(L1 + b/2,0), box.p1 + db.DPoint(dx -␣
 ↪(L1+b/2), 0), box.p2 - db.DPoint(L1 + b/2, 0),  box.p1 + db.DPoint(L1 + b/2,␣
 ↪dy)]

# Define several layers as a test. You can create as many as you want as long␣
 ↪as they are numbered differently
layer_info_photo = db.LayerInfo(10, 0,'Resonator') # main resonator design
layer_crosses = db.LayerInfo(2, 0, 'Boundaries') # used for crosses marking␣
 ↪chip boundaries
layer_negative = db.LayerInfo(4, 0, 'Negative') # used for ???

layer_photo = layout.layer(layer_info_photo)
layer_cross = layout.layer(layer_crosses)
layer_neg = layout.layer(layer_negative)
```

1.2 Set parameters

Set parameters for: materials, feedline geometry, resonator number and geometry

[3]:
```
'''Wafer'''
wafer_x = 20000e3
wafer_y = wafer_x
min_border = 700e3

'''Chips'''
N_repetitions = 7 # number of repetitions in y (top and bottom row will be test␣
 ↪feature chips)
chip_x_gap = 0 # horizontal chip gap
chip_y_gap = 0 # vertical chip gap
```

```
'''Substrate Material'''
er = 8.325 # relative permittivity of substrate

'''Feedline'''
width = 18e3 # Conductor width
gap = 6e3 # Substrate gap
fraction = 8.5/10 # Feedline y pos. on chip

'''Contacts'''
contact_L = 550e3   # Adapter length
width_launcher = 200e3 # Launcher width (gap scaled as CPW gap)
length_launcher = 400e3 # Launcher length

'''Resonators'''
N_bottom = 5 # Number of resonators
coupling_length = 100 # Coupling lengths - resonator/feedline coupling (in um)
L_coupling = list(map( lambda x: x * 1e3, [coupling_length] * N_bottom )) #␣
 ↪creates list of couple lengths in nm set by coupling_length
L1 = np.linspace(310e3, 680e3, N_bottom) # Main length across resonator (300um␣
 ↪for left most res, up to 600um for right most res)
r = 70e3 # Turn radius
L2 = 100e3 # Open end length (vertical section on bottom of resonators)
N_turns = 3 # Number of turns in the resonator
toLine = 37e3 #equiv. to 36um (not accurate) # Distance between resonator and␣
 ↪feedline (check distance in klayout - not fully accurate)
width_res = width # Width of the resonator (currently equal to main feedline␣
 ↪CPW)
gap_res = gap # Gap between center and ground planes
res_shift_x = 350e3 # Horizontal displacement of first resonator

'''Markers'''
cross_small = 20e3 # Cross2()
cross_small_neg = 100e3
cross_large = 500e3
cross_large_neg = 550e3

'''Feature Chips'''
upscale = 1.5e3 # sets multiplier for each consequent feature (i.e. arcs,␣
 ↪windows)
num_feature_chips = 4 # number of feature chips
num_features = 3 # number of CPW per feature chip
feature_chip_border = 100e3
feature_xgap = 200e3 # horizontal gap between features
feature_gap = 6e3 # min gap
feature_width = feature_gap # min width
num_arcs = 21 # ARC parameters
```

```
arc_radius = 0.5e5
arc_gap_V = toLine * 2
arc_gap_H = 5e5
num_windows = 70 # WINDOW parameters
upscale2 = 1e3
window_dimension_init = 2e3
```

2 Draw Geometries

Let us draw the basic chip with crosses to delimit its boundaries.

The next cell defines the number of repetitions of the chip design that you would like to do. If N_repetitions is greater than 1, you also have a list of relative origins for each repetition of the chip in origins. Consider whether you would like to create this repetitions in the code or just copy them directly in KLayout.

It also defines a DPoint and Vector versions of the origin, since different classes may use both of them.

Finally, it creates the basic chip geometry in the layer_photo layer.

[4]:
```
# Design: N_repitions in number of chips in y-direction
# All design have two columns of chips -> total chip number = N_repetitions * 2

# Draw wafer
origin = db.DPoint(0, 0)
cell.shapes(layer_photo).insert(db.Box(origin, Point(0 + wafer_x, 0 + wafer_y)))

# Calculate borders, check for errors
wafer_border_x = (wafer_x - (CHIP.dx * 2))/2 # size of no-print-zone around␣
 ↪edge of wafer
wafer_border_y = (wafer_y - (N_repetitions * CHIP.dy))/2 # size of␣
 ↪no-print-zone around edge of wafer
if (N_repetitions * CHIP.dy) > (wafer_y - (min_border*2)):
    print("Too many chips!")
    exit()

'''Define origins as list (not DPoint)'''
Origin_list = [(0*CHIP.dx + wafer_border_x, n*(CHIP.dy + chip_y_gap) +␣
 ↪wafer_border_y)for n in range(N_repetitions)] # column 1
Origin_list_dx = [(1*CHIP.dx + chip_x_gap + wafer_border_x, n*(CHIP.dy +␣
 ↪chip_y_gap) + wafer_border_y)for n in range(N_repetitions)] # column 2
for i in range(N_repetitions):
    Origin_list.append(Origin_list_dx[i])
# print(f"Origins [nm]: {Origin_list}") # [uncomment to print origin list]

# Set origin to nth location in Origin_list, create origin vector
for n in range(N_repetitions*2):
```

```
    # setup origin for n'th chip
    origins = Origin_list[n] # take nth origin from Origin_list to convert to␣
↪DPoint
    origin = db.DPoint(origins[0], origins[1]) # convert to DPoint
    Origin_V = Vector(origins[0], origins[1]) # convert to Vector
    cell.shapes(layer_photo).insert(db.Box(origin, Point(origins[0] + 1*CHIP.
↪dx, origins[1] + 1*CHIP.dy )))

    '''Draw markers (crosses)'''
    # On 'Boundaries' layer
    cross_ll = Cross2(Origin_V, cross_small, cross_large)
    cross_ll.place(cell, layer_cross)
    cross_lr = Cross2(Origin_V + Vector(1*CHIP.dx, 0), cross_small, cross_large)
    cross_lr.place(cell, layer_cross)
    cross_ul = Cross2(Origin_V + Vector(0, 1*CHIP.dy), cross_small, cross_large)
    cross_ul.place(cell, layer_cross)
    cross_ur = Cross2(Origin_V + Vector(1*CHIP.dx, 1*CHIP.dy), cross_small,␣
↪cross_large)
    cross_ur.place(cell, layer_cross)
    # On 'Negatives' layer
    cross_ll = Cross2(Origin_V, cross_small_neg, cross_large_neg)
    cross_ll.place(cell, layer_neg)
    cross_lr = Cross2(Origin_V + Vector(1*CHIP.dx, 0), cross_small_neg,␣
↪cross_large_neg)
    cross_lr.place(cell, layer_neg)
    cross_ul = Cross2(Origin_V + Vector(0, 1*CHIP.dy), cross_small_neg,␣
↪cross_large_neg)
    cross_ul.place(cell, layer_neg)
    cross_ur = Cross2(Origin_V + Vector(1*CHIP.dx, 1*CHIP.dy), cross_small_neg,␣
↪cross_large_neg)
    cross_ur.place(cell, layer_neg)

    '''Draw feature chips'''
    if n < num_feature_chips:

        # Set 'feature length' from chosen feature parameters
        feature_length = (CHIP.dx - ((num_features-1) * feature_xgap)
                          - (feature_chip_border * 2)) / num_features

        # shift origin up slightly (due to the way feature writing is␣
↪programmed)
        origin = origin + db.DPoint(feature_chip_border, CHIP.dy/2 + 250e3)
        '''CPW 1'''
        p7 = origin
        p8 = origin + DPoint(feature_length, 0)
```

```
        F1 = CPW(feature_width, feature_gap, p7, p8)
        F1.place(cell, layer_photo)
        '''CPW 2'''
        p9 = F1.end + DPoint(feature_xgap, 0)
        p10 = p9 + DPoint(feature_length, 0)
        F2 = CPW(feature_width*2, feature_gap*2, p9, p10)
        F2.place(cell, layer_photo)
        '''CPW 3'''
        p11 = F2.end + DPoint(feature_xgap, 0)
        p12 = p11 + DPoint(feature_length, 0)
        F3 = CPW(feature_width*3, feature_gap*3, p11, p12)
        F3.place(cell, layer_photo)
        '''Arcs'''
        arcs = []
        new_origin = origin - DPoint(-arc_gap_H/2, arc_gap_V)
        point = new_origin
        for i in range(num_arcs):
            # Scale radius and gap/width for each arc
            arcR = arc_radius + (2 * i * upscale)
            F1.width = feature_width + (i * upscale)
            F1.gap = feature_gap + (i * upscale)
            # Add new arc to list
            arcF = CPW_arc(F1, point, -arcR, -2*np.pi)
            arcF.place(cell, layer_photo)
            arcs.append(arcF)
            # Adjust start point
            point = new_origin + DPoint(arcR + arc_gap_H, -F1.gap/4)
            arc_gap_H = arc_gap_H + (upscale*2)
            new_origin = point
            if new_origin.x > (origin.x + CHIP.dx - (2 * arcR)):
                break
        '''Windows'''
        windows = []
        window_origin = origin - DPoint(-arc_gap_H/2, arc_gap_V * 5)
        point2 = window_origin
        for i in range(num_windows):
            # Scale width/height for each window
            window_dimension = window_dimension_init + (i * upscale2)
            # Add new arc to list
            windowF = Rectangle(window_origin, window_dimension,␣
↪window_dimension, inverse=True)
            windowF.place(cell, layer_photo)
            windows.append(windowF)
            # Adjust start point
            window_origin = point2 + DPoint(200e3*i, 0)
            if window_origin.x > (origin.x + CHIP.dx - window_dimension):
                break
```

```
    else:

        '''Draw feedline elements'''
        # Central CPW feedline (straight part)
        p1 = origin + DPoint( 0 + length_launcher + contact_L, CHIP.dy*fraction␣
↪)
        p2 = origin + DPoint( CHIP.dx - length_launcher - contact_L, CHIP.
↪dy*fraction )
        Z0 = CPW( width, gap, p1, p2 )
        Z0.place( cell, layer_photo )
        ### LEFT SIDE
        # Left contact pads (big rectangles on left side) - defined as wider␣
↪CPW vertically centered on chip
        gap_launcher = width_launcher/width*gap
        p3 = origin + DPoint( 0, CHIP.dy/2 )
        p4 = origin + DPoint( length_launcher, CHIP.dy/2 )
        Z1 = CPW( width_launcher, gap_launcher, p3, p4 )
        Z1.place( cell, layer_photo )
        # CPW left top arc
        arc1 = CPW_arc(Z0, p1, -1.0e5, np.pi/2)
        arc1.place(cell, layer_photo)
        # CPW left vertical
        Z3 = CPW(Z0.width, Z0.gap, arc1.end, DPoint(0, origins[1]+CHIP.dy/2) +␣
↪DPoint(arc1.end.x, 1e5))
        Z3.place(cell, layer_photo)
        # CPW left horizontal into adapters
        Z4 = CPW(Z0.width, Z0.gap, Z3.end - DPoint(1.0e5, 1.0e5), Z3.end -␣
↪DPoint(1.5e5,1.0e5))
        Z4.place(cell, layer_photo)
        # CPW left bottom arc
        arc2 = CPW_arc(Z0, Z4.start, 1.0e5, np.pi/2)
        arc2.place(cell, layer_photo)
        # Adapter between left launcher and the central feedline CPWs, which␣
↪will bridge them together
        adapter1 = CPW2CPW( Z1, Z0, p4, Z4.end )
        adapter1.place( cell, layer_photo )
        ### RIGHT SIDE
        # Right contact pads
        p5 = origin + DPoint( CHIP.dx - length_launcher, CHIP.dy/2 )
        p6 = origin + DPoint( CHIP.dx, CHIP.dy/2 )
        Z2 = CPW( width_launcher, gap_launcher, p5, p6 )
        Z2.place( cell, layer_photo )
        # CPW right top arc
        arc3 = CPW_arc(Z0, p2, -1.0e5, -np.pi/2)
        arc3.place(cell, layer_photo)
        # CPW right vertical
```

```
        Z5 = CPW(Z0.width, Z0.gap, arc3.end, DPoint(0, origins[1] + CHIP.dy/
↪2)+DPoint(arc3.end.x, 1e5))
        Z5.place(cell, layer_photo)
        # CPW right short horizontal into adapters
        Z6 = CPW(Z0.width, Z0.gap, Z5.end + DPoint(1.0e5, -1.0e5), Z5.end +␣
↪DPoint(1.5e5,-1.0e5))
        Z6.place(cell, layer_photo)
        # CPW right bottom arc
        arc4 = CPW_arc(Z0, Z6.start, 1.0e5, -np.pi/2)
        arc4.place(cell, layer_photo)
        # Adapter between right launcher and the central feedline CPWs, which␣
↪will bridge them together
        adapter2 = CPW2CPW( Z2, Z0, p5, Z6.end )
        adapter2.place( cell, layer_photo )

        '''Draw resonator elements'''
        # Define the CPW
        Z_res = CPW( width_res, gap_res, origin, origin )
        # Separation between resonators along x
        delta = 0.3*CHIP.dx/4
        if N_bottom >1:
            step_bot = (CHIP.dx - 2*contact_L - 2*delta)/(N_bottom-1)
        else:
            step_bot = (CHIP.dx - 2*contact_L - 2*delta)
        resonators = []
        res_lengths = []
        # Draw resonators along bottom of feedline
        for i in range( N_bottom ):
            # Define the point for the shorted part of the resonator to begin
            point = origin + DPoint( contact_L + delta + i*2*delta +␣
↪res_shift_x, CHIP.dy*fraction - ((Z0.width + Z_res.width+50e3)/2 + toLine)  )
            # Create the resonator and place it in the main layer
            worm = EMResonator_worm(Z_res, point, L_coupling[i], L1[i], r, L2,␣
↪N_turns)
            worm.place( cell, layer_photo )
            # Append each resonator to the list of resonators
            resonators.append( worm )
            # Calculate resonator lengths
            res_length = L_coupling[i] + ( L1[i]*(N_turns*2+1) ) + L2 + ( np.
↪pi*r*(N_turns*2+2) ) + (np.pi*L1[i]/4)
            res_lengths.append( res_length/1e3 )

    print(f"Chip {n} printed")
print("Done!")
```

```
Chip 0 printed
Chip 1 printed
```

```
Chip 2 printed
Chip 3 printed
Chip 4 printed
Chip 5 printed
Chip 6 printed
Chip 7 printed
Chip 8 printed
Chip 9 printed
Chip 10 printed
Chip 11 printed
Chip 12 printed
Chip 13 printed
Done!
```

The next cell draws the feedline, contacts and resonators based on parameters set above.

[5]:
```
# Print resonator lengths in um and resonance frequencies
c = 299792458.0 # speed of light in m/s
cl = c / np.sqrt(er/2 + 0.5) # speed of light in medium (substrate) sqrt((er +␣
↪(e0/e0)/2)
print(f"Substrate relative permittivity = {er}\nGap/Width [nm] = {gap}/{width}")
print(f"++++ Resonators ++++ \nResonator lengths [um]: {res_lengths}")
res_freqs = [(cl/(4*i/1e6)) / 1e9 for i in res_lengths]
print(f"Resonant frequencies [GHz]: {res_freqs}")
```

```
Substrate relative permittivity = 8.325
Gap/Width [nm] = 6000.0/18000.0
++++ Resonators ++++
Resonator lengths [um]: [4372.765316663494, 5092.914646777756,
5813.063976892021, 6533.213307006285, 7253.362637120548]
Resonant frequencies [GHz]: [7.937708014479712, 6.815298646616684,
5.970987836620446, 5.31281203727049, 4.785330064966648]
```

[6]:
```
# change to directory for writing files, write file (defined in cell 1)
os.chdir(printpath)
layout.write(filename)

# change back to original path
os.chdir(working_path)
```

A.2 High resolution XPS scans of the MAO substrate before and after surface treatment

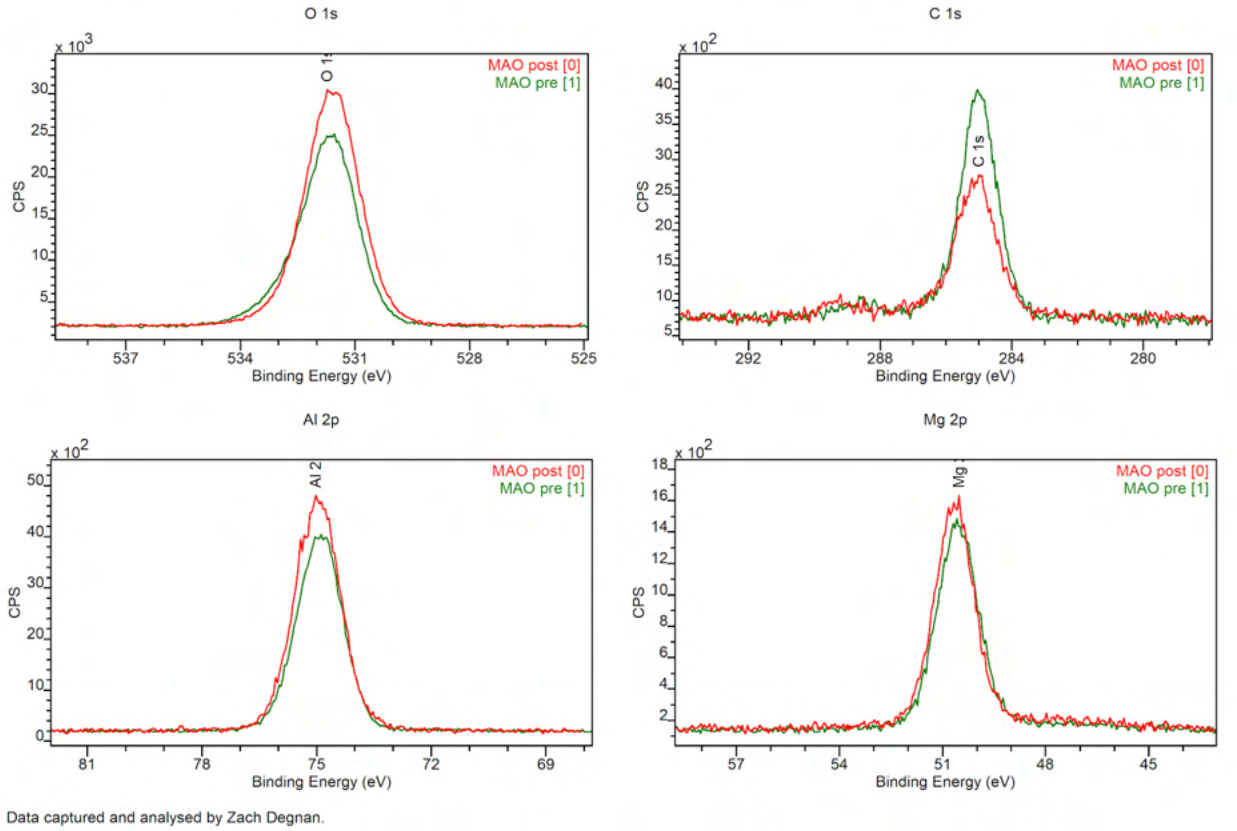


Figure A.1: Normalised high resolution XPS scans of the characteristic XPS peaks for MAO. The data corresponding to the untreated substrate is shown in green, whilst the treated substrate corresponds to the red data. We can see that the concentrations of native MAO atoms are boosted, and the carbon contamination is reduced after surface treatment.

A.3 Measurements script and example Q-factor fits for MAO resonators

Here, the scripts used for measurement and fitting of MAO Q-factors are displayed. We also show the power-dependence plots with a linear y-scale, and an example high and low power fit, as performed by Probst's circle fit algorithm [5].

MAOpower_thesis

June 2, 2021

1 Q vs. Power - MAO

1.0.1 Power fit for all 5 resonators

[22]:
```
# Load packages

#import uqtools as uq # https://github.com/sqdlab/uqtools
from resonator_tools import circuit # https://github.com/sebastianprobst/
 ↪resonator_tools/tree/master/resonator_tools
import sys
import numpy as np
import matplotlib.pyplot as plt
import time
import os
import matplotlib
from scipy.optimize import curve_fit
from numpy import loadtxt

%matplotlib inline
# uq.config.datadir = r'Z:\\Data (eqlab3)'
```

2 Power dependence plotting and fitting

Reads directly from saved text files

[23]:
```
num_resonators = 5
freqs = [4.80555e9, 5.3143e9, 5.9685e9, 6.84089e9, 7.98434e9] # Hz

Qs = []
Q_err = []
n_ph = []

# read in sorted data from text files
os.chdir('/Volumes/EQUS-SQDLab/PEOPLE/Zach_D/Resonators/Data/MAO_Q')

# individual resonators to seperate file - full power sweep
for i in range(num_resonators):
```

```
    freq_format = '{:.1e}'.format(freqs[i])

    print('MAO_{}GHz_sorted.txt'.format(freq_format))

    f_cur = 'MAO_{}GHz_sorted.txt'.format(freq_format)
    with open(f_cur,'r') as f:
        n_ph.append(loadtxt(f_cur, comments='#', usecols=1))
        Qs.append(loadtxt(f_cur, comments='#', usecols=2))
        Q_err.append(loadtxt(f_cur, comments='#', usecols=3))
# Qs, Q_err, and n_ph arrays now populated

# save Q_H (n_ph=2000) and Q_L (n_ph = 1) for each resonator to file
f = open('MAO_Q_summary.txt'.format(freqs[i]), 'w') # open file
f.write("#f [Hz]\t\tQ_H\t\tn_H\t\tQ_L\t\tn_L\n") # header

QHindex = 42
QLindex = 9
N = len(Qs[0])

# print Q_H, Q_L values to file
# f     Q_H   n_H    Q_L    n_L
for i in range(num_resonators):
    f.write('Done - next res \n{}\n'.format(freqs[i]))
    freq = freqs[i]
    for j in range(N):
        if (j == QHindex):
            QH = Qs[i][j]
            QH_err = Q_err[i][j]
            n_H = n_ph[i][j]
            f.write('\n    {}+/-{}\n{}\n'.format(Qs[i][j], Q_err[i][j],␣
 ↪n_ph[i][j]))
        elif (j == QLindex):
            QL = Qs[i][j]
            QL_err = Q_err[i][j]
            n_L = n_ph[i][j]
            f.write('      {}+/-{}\n{}\n'.format(Qs[i][j], Q_err[i][j],␣
 ↪n_ph[i][j]))
        else:
            continue
        #f.write('{:.1e}\t{:.1e}+\-{:.1e}\t{:.1e}\t{:.1e}+\-{:.1e}\t{:.1e}\n'.
 ↪format(freq, QH, QH_err, n_H, QL, QL_err, n_L))

f.write('Done!')
f.close()
```

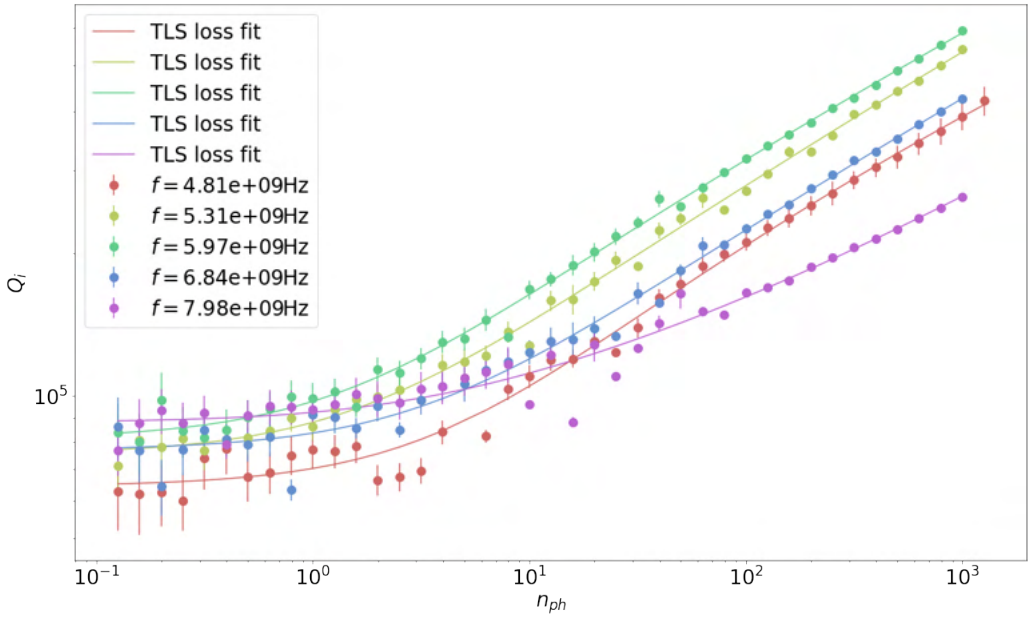
```
MAO_4.8e+09GHz_sorted.txt
MAO_5.3e+09GHz_sorted.txt
```

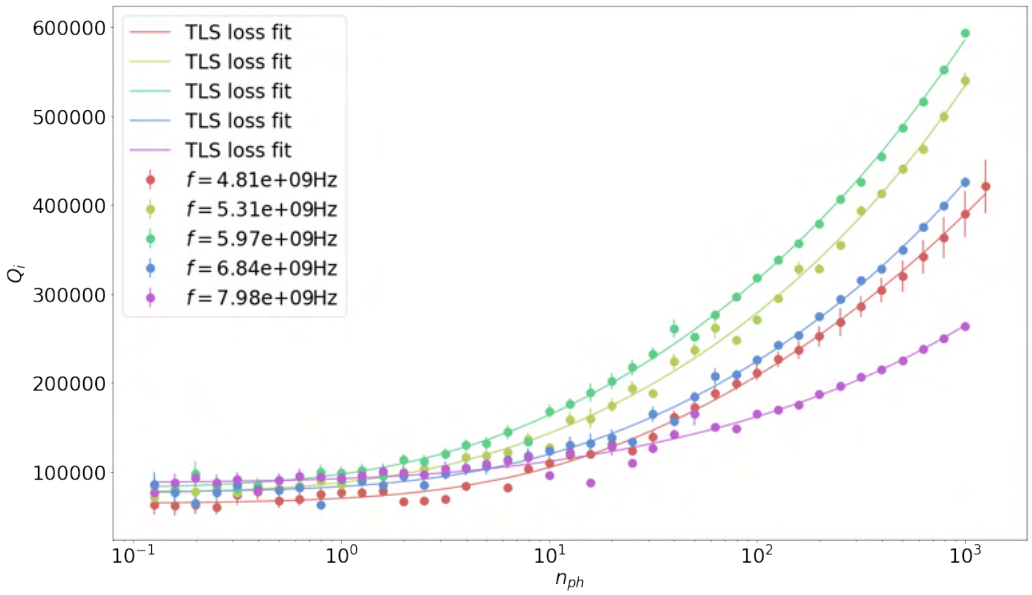
```
MAO_6.0e+09GHz_sorted.txt
MAO_6.8e+09GHz_sorted.txt
MAO_8.0e+09GHz_sorted.txt
```

3 Plot and TLS loss fit

[24]:
```
# TLS loss fit
def TLSloss(n_ph, F, Q_TLS, n_c, beta, other_losses):
    quotient = (1 + (np.array(n_ph) / n_c)) ** beta
    frac = 0.99297056429 / quotient # where the scalar is the value of tanh(A*T)
    return (F * (1 / Q_TLS) * frac + other_losses)


# setup colours
import colorsys
N = 5
HSV_tuples = [(x*1.0/N, 0.5, 0.8) for x in range(N)]
colors = list(map(lambda x: colorsys.hsv_to_rgb(*x), HSV_tuples))

# trim last few terms of arrays
trim = 40

# plot 1 : x log, y log
fig = plt.gcf()
fig.set_size_inches(20, 12, forward=True)
matplotlib.rcParams.update({'font.size': 24})

#for i in range(num_resonators):
for i in range(num_resonators):

    # trim arrays
    Qs[i] = Qs[i][:trim]
    Q_err[i] = Q_err[i][:trim]
    n_ph[i] = n_ph[i][:trim]

    # plot 1: log-log
    plt.errorbar(n_ph[i], Qs[i], yerr=Q_err[i], linestyle="None", marker=".",
                 markersize=20, label="$f=${:.2e}Hz".
 ↪format(freqs[i]),c=colors[i])
    popt2, pcov2 = curve_fit(TLSloss, n_ph[i], Qs[i])
    plt.plot(n_ph[i], TLSloss(n_ph[i], *popt2), label='TLS loss␣
 ↪fit',c=colors[i])
    plt.xlabel('$n_{ph}$')
    plt.ylabel('$Q_i$')
    plt.xscale('log')
    plt.yscale('log')
    plt.legend()
```

```
    # plt.show()
    # fig.savefig('MAO{:.1e}Hz_log.png'.
↪format(freqs[i]),facecolor='w',transparent=False)

# plot and save
plt.show()
fig.savefig('MAO_Qfit_log.png',facecolor='w',transparent=False)

for i in range(num_resonators):

    # plot 2 : log-linear
    popt2, pcov2 = curve_fit(TLSloss, n_ph[i], Qs[i])
    plt.plot(n_ph[i], TLSloss(n_ph[i], *popt2), c=colors[i], label='TLS loss␣
↪fit')
    fig = plt.gcf()
    fig.set_size_inches(20, 12, forward=True)
    matplotlib.rcParams.update({'font.size': 24})
    plt.errorbar(n_ph[i], Qs[i], yerr=Q_err[i], linestyle="None", marker=".",
                 markersize=20, label="$f=${:.2e}Hz".format(freqs[i]),␣
↪c=colors[i])
    plt.xlabel('$n_{ph}$')
    plt.ylabel('$Q_i$')
    plt.legend()
    plt.xscale('log')
    plt.yscale('linear')
    #plt.show()
    # fig.savefig('MAO{:.1e}Hz_linear.png'.
↪format(freqs[i]),facecolor='w',transparent=False)

# plot and save
plt.show()
fig.savefig('MAO_Qfit_lin.png',facecolor='w',transparent=False)
```


TLS loss fit
TLS loss fit
TLS loss fit
TLS loss fit
TLS loss fit
f = 4.81e+09Hz
f = 5.31e+09Hz
f = 5.97e+09Hz
f = 6.84e+09Hz
f = 7.98e+09Hz
Q_i
10^5
10^{-1}
10^0
10^1
10^2
10^3
n_{ph}


TLS loss fit
TLS loss fit
TLS loss fit
TLS loss fit
TLS loss fit
f = 4.81e+09Hz
f = 5.31e+09Hz
f = 5.97e+09Hz
f = 6.84e+09Hz
f = 7.98e+09Hz
Q_i
600000
500000
400000
300000
200000
100000
10^{-1}
10^0
10^1
10^2
10^3
n_{ph}

Power loops

In [13]:
```
power = uq.Parameter('power')
power.set(0)
```

In [14]:
```
frequencies = uq.Parameter('frequencies')
frequencies.set(4e9)
```

In [15]:
```
bandwidth = uq.Parameter('bandwidth')
bandwidth.set(100)
```

In [16]:
```
class VNATrace(uq.Measurement):
    def _measure(self, *args, **kwargs):
        vna.SetupLinearSweep('S42',
                     freq_start=frequencies.get() - 0.6e6,
                     freq_stop=frequencies.get() + 0.5e6,
                     sweep_points=401,
                     power=power.get(),
                     averages = 50)
        vna.bandwidth(bandwidth.get())
        vna.averaging(1)
        frame =  vna.get_trace_raw()
        self.store.append(frame)
        return frame
```

In [1]:
```
# resonator frequencies
freqs = [4.80555e9, 5.3143e9, 5.9685e9, 6.84089e9, 7.98434e9] # MAO

# manual attenuation
manual_atten =  -120 # 60 dB in fridge, 50 outside, 10 in cables

# taking measurements for all resonators at 3 power levels
for freq in freqs:
    for pwr in np.arange(16, -31, -1):
        if pwr > 0:
            bandwidth.set(300)
        elif (pwr <= -0 and pwr > -10):
            bandwidth.set(200)
        else:
            bandwidth.set(100)
        print(pwr, bandwidth.get())
        frequencies.set(freq)
        power.set(pwr)
        vnam = VNATrace(name = f'Resonator_{frequencies.get()}_GHz_{power.get()+manual_atten}_dBm')
        source = vnam(output_data = True)
        #source
```

Figure A.2: A section of the script used to perform VNA measurements in Assoc. Prof. Arkady Federov's lab at UQ (SQD Lab).

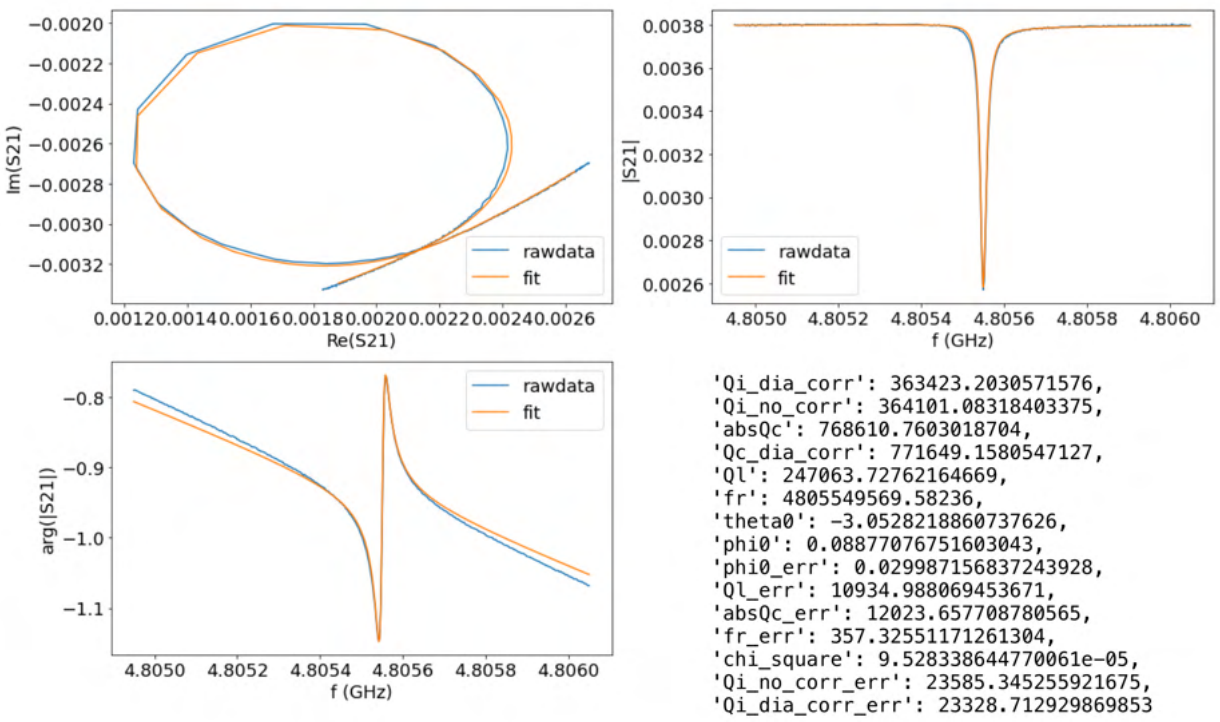


FIGURE A.3: S_{21} transmission of the 4.8GHz resonator on the MAO chip at high power ($\langle n_{ph} \rangle \approx 2000$). The extracted fit values are listed in the bottom right of the figure. The internal Q-factor with environmental corrections is listed as `Qi_dia_corr`.

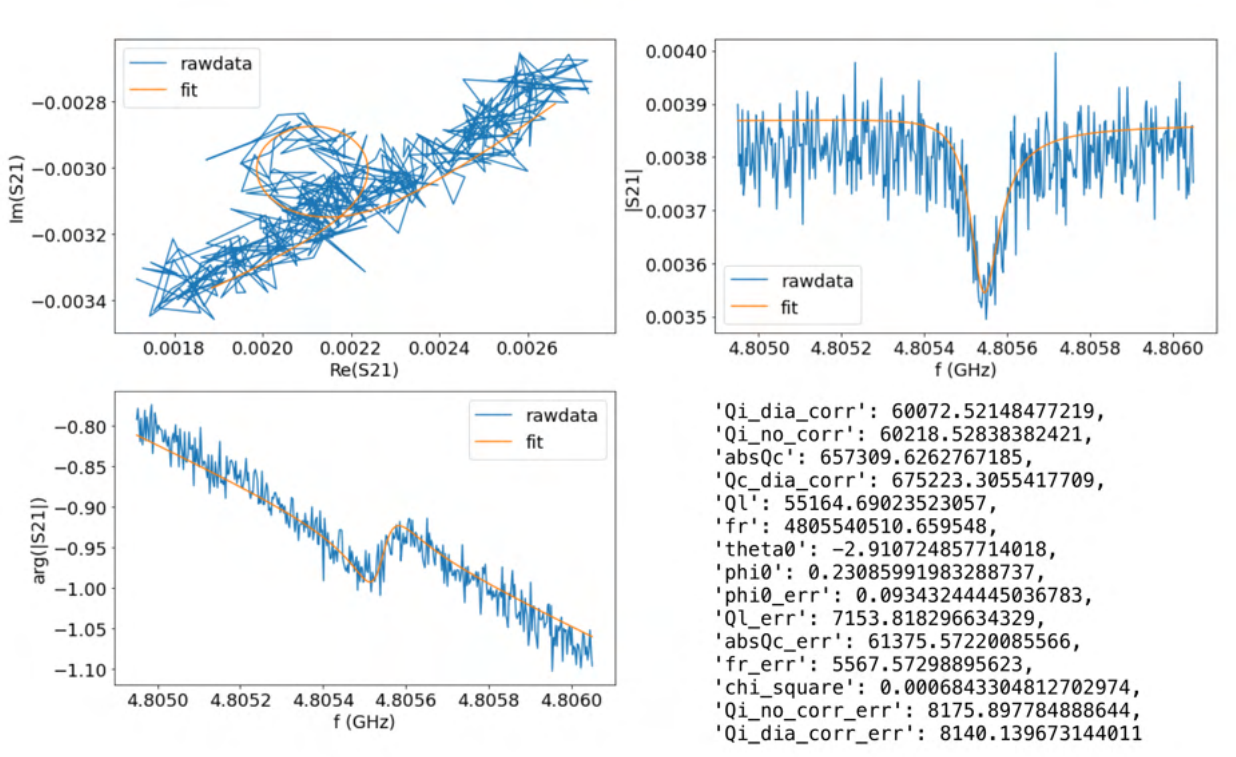


Figure A.4: S_{21} transmission of the 4.8GHz resonator on the MAO chip at low power ($\langle n_{ph} \rangle \approx 1$). Fit details the same as those given in figure A.3.

References

[1] C. Müller, J. H. Cole, and J. Lisenfeld. *Towards understanding two-level-systems in amorphous solids: Insights from quantum circuits.* Reports on Progress in Physics **82**(12), 124501 (2019). URL https://iopscience.iop.org/article/10.1088/1361-6633/ab3a7e.

[2] R. Barends, J. Kelly, A. Megrant, D. Sank, E. Jeffrey, Y. Chen, Y. Yin, B. Chiaro, J. Mutus, C. Neill, P. O'Malley, P. Roushan, J. Wenner, T. C. White, A. N. Cleland, and J. M. Martinis. *Coherent Josephson Qubit Suitable for Scalable Quantum Integrated Circuits.* Physical Review Letters **111**(8), 080502 (2013). URL https://link.aps.org/doi/10.1103/PhysRevLett.111.080502.

[3] C. Beydeda. *Superconducting Flip-Chip Microwave Resonators on Materials with High Dielectric Constant.* Ph.D. thesis, Physikalisches Institut Universität Stuttgart, Stuttgard, Germany (2020).

[4] V. T. Engl and M. Dressel. *Planar Microwave Resonators on SrTiO 3 Substrates.* Ph.D. thesis (2019). URL /paper/Planar-microwave-resonators-on-SrTiO-3-substrates-Engl-Dressel/c3b87eab49685fd531b06b4f74be08411d8c7ed5.

[5] S. Probst, F. B. Song, P. A. Bushev, A. V. Ustinov, and M. Weides. *Efficient and robust analysis of complex scattering data under noise in microwave resonators.* Review of Scientific Instruments **86**(2), 024706 (2015). URL http://aip.scitation.org/doi/10.1063/1.4907935.

[6] J. Burnett, A. Bengtsson, D. Niepce, and J. Bylander. *Noise and loss of superconducting aluminium resonators at single photon energies.* Journal of Physics: Conference Series **969**, 012131 (2018). URL https://iopscience.iop.org/article/10.1088/1742-6596/969/1/012131.

[7] R. Kennedy and P. Stampe. *The influence of lattice mismatch and film thickness on the growth of TiO2 on LaAlO3 and SrTiO3 substrates.* Journal of Crystal Growth **252**(1-3), 333 (2003). URL https://linkinghub.elsevier.com/retrieve/pii/S0022024802025149.

[8] *Silicon Based Epitaxial Thin Films* (2021). URL https://www.mksinst.com/n/silicon-epitaxial-thin-films.

[9] F. J. Giessibl. *Forces and frequency shifts in atomic-resolution dynamic-force microscopy*. Physical Review B **56**(24), 16010 (1997). URL https://link.aps.org/doi/10.1103/PhysRevB.56.16010.

[10] T. Herden. *Design and Construction of a Q-Sensor AFM/STM for Low Temperatures*. Ph.D. thesis, Physics Department, University of Konstanz and Max Planck Institute for Solid State Research, Stuttgart (2010).

[11] *CasaXPS Orange Book* (2008). URL http://www.casaxps.com/ebooks/OrangeBookRev1.3ebook.pdf.

[12] M. Yasaka. *X-ray thin-film measurement techniques* p. 9 (2010).

[13] A. Biswas, C.-H. Yang, R. Ramesh, and Y. H. Jeong. *Atomically flat single terminated oxide substrate surfaces*. Progress in Surface Science **92**(2), 117 (2017). URL https://linkinghub.elsevier.com/retrieve/pii/S0079681617300114.

[14] J. E. Kleibeuker, G. Koster, W. Siemons, D. Dubbink, B. Kuiper, J. L. Blok, C.-H. Yang, J. Ravichandran, R. Ramesh, J. E. ten Elshof, D. H. A. Blank, and G. Rijnders. *Atomically Defined Rare-Earth Scandate Crystal Surfaces*. Advanced Functional Materials **20**(20), 3490 (2010). URL http://doi.wiley.com/10.1002/adfm.201000889.

[15] I. Besedin and A. P. Menushenkov. *Quality factor of a transmission line coupled coplanar waveguide resonator*. EPJ Quantum Technology **5**(1), 2 (2018). URL https://epjquantumtechnology.springeropen.com/articles/10.1140/epjqt/s40507-018-0066-3.

[16] *Nitto SWT 10T+R Datasheet* (2021). URL https://www.nitto.com/au/en/others/products/file/datasheet/NBE_SWT%2010T+R_EN.pdf.

[17] *ADT Dicing Blades & Accessories*. URL https://www.adt-co.com/uploads/img/20200623/569c5c97868c9e755d2d2c94b1cc1f35.pdf.

[18] *TPT HB16 Wedge & Ball Bonder: Datasheet*. URL https://www.tpt-wirebonder.com/wp-content/uploads//00_Media/99_Elemente_und_Platzhalter/Datenbl%C3%A4tter/HB16_Datasheet_2020.pdf.

[19] *Australian National Fabrication Facility – Queensland Node (ANFF-Q)*. URL https://anff-q.org.au/.

[20] A. Nelson. *Co-refinement of multiple-contrast neutron/X-ray reflectivity data using* MOTOFIT. Journal of Applied Crystallography **39**(2), 273 (2006). URL http://scripts.iucr.org/cgi-bin/paper?S0021889806005073.

[21] P. Krantz, M. Kjaergaard, F. Yan, T. P. Orlando, S. Gustavsson, and W. D. Oliver. *A quantum engineer's guide to superconducting qubits*. Applied Physics Reviews **6**(2), 021318 (2019). URL http://aip.scitation.org/doi/10.1063/1.5089550.

[22] C. R. H. McRae, H. Wang, J. Gao, M. R. Vissers, T. Brecht, A. Dunsworth, D. P. Pappas, and J. Mutus. *Materials loss measurements using superconducting microwave resonators*. Review of Scientific Instruments **91**(9), 091101 (2020). URL http://aip.scitation.org/doi/10.1063/5.0017378.

[23] S. Probst. *GitHub Repository: Resonator Tools* (2020). URL https://github.com/sebastianprobst/resonator_tools.

[24] C. Neill, P. Roushan, K. Kechedzhi, S. Boixo, S. V. Isakov, V. Smelyanskiy, A. Megrant, B. Chiaro, A. Dunsworth, K. Arya, R. Barends, B. Burkett, Y. Chen, Z. Chen, A. Fowler, B. Foxen, M. Giustina, R. Graff, E. Jeffrey, T. Huang, J. Kelly, P. Klimov, E. Lucero, J. Mutus, M. Neeley, C. Quintana, D. Sank, A. Vainsencher, J. Wenner, T. C. White, H. Neven, and J. M. Martinis. *A blueprint for demonstrating quantum supremacy with superconducting qubits*. Science **360**(6385), 195 (2018). URL https://www.sciencemag.org/lookup/doi/10.1126/science.aao4309.

[25] M. A. Nielsen and I. L. Chuang. *Quantum Computation and Quantum Information* (Cambridge University Press, Cambridge ; New York, 2010), 10th anniversary ed ed.

[26] W. Huang, C. H. Yang, K. W. Chan, T. Tanttu, B. Hensen, R. C. C. Leon, M. A. Fogarty, J. C. C. Hwang, F. E. Hudson, K. M. Itoh, A. Morello, A. Laucht, and A. S. Dzurak. *Fidelity benchmarks for two-qubit gates in silicon*. Nature **569**(7757), 532 (2019). URL http://www.nature.com/articles/s41586-019-1197-0.

[27] C. D. Bruzewicz, J. Chiaverini, R. McConnell, and J. M. Sage. *Trapped-ion quantum computing: Progress and challenges*. Applied Physics Reviews **6**(2), 021314 (2019). URL http://aip.scitation.org/doi/10.1063/1.5088164.

[28] J. Q. You and F. Nori. *Atomic physics and quantum optics using superconducting circuits*. Nature **474**(7353), 589 (2011). URL http://www.nature.com/articles/nature10122.

[29] J. Burnett, L. Faoro, and T. Lindström. *Analysis of high quality superconducting resonators: Consequences for TLS properties in amorphous oxides*. Superconductor Science and Technology **29**(4), 044008 (2016). URL https://iopscience.iop.org/article/10.1088/0953-2048/29/4/044008.

[30] M. V. P. Altoé, A. Banerjee, C. Berk, A. Hajr, A. Schwartzberg, C. Song, M. A. Ghadeer, S. Aloni, M. J. Elowson, J. M. Kreikebaum, E. K. Wong, S. Griffin, S. Rao, A. Weber-Bargioni, A. M. Minor, D. I. Santiago, S. Cabrini, I. Siddiqi, and D. F. Ogletree. *Localization and reduction of superconducting quantum coherent circuit losses*. arXiv:2012.07604 [cond-mat, physics:quant-ph] (2020). 2012.07604, URL http://arxiv.org/abs/2012.07604.

[31] J. Burnett, L. Faoro, I. Wisby, V. L. Gurtovoi, A. V. Chernykh, G. M. Mikhailov, V. A. Tulin, R. Shaikhaidarov, V. Antonov, P. J. Meeson, A. Y. Tzalenchuk, and

T. Lindstrom. *Evidence for interacting two-level systems from the 1/f noise of a superconducting resonator*. Nature Communications **5**(1), 4119 (2014). 1311.1655, URL http://arxiv.org/abs/1311.1655.

[32] J. M. Martinis, K. B. Cooper, R. McDermott, M. Steffen, M. Ansmann, K. Osborn, K. Cicak, S. Oh, D. P. Pappas, R. W. Simmonds, and c. C. Yu. *Decoherence in Josephson Qubits from Dielectric Loss*. Physical Review Letters **95**(21), 210503 (2005). cond-mat/0507622, URL http://arxiv.org/abs/cond-mat/0507622.

[33] J. Tournet, D. Gosselink, G.-X. Miao, M. Jaikissoon, D. Langenberg, T. G. McConkey, M. Mariantoni, and Z. R. Wasilewski. *Growth and characterization of epitaxial aluminum layers on gallium-arsenide substrates for superconducting quantum bits*. Superconductor Science and Technology **29**(6), 064004 (2016). URL https://iopscience.iop.org/article/10.1088/0953-2048/29/6/064004.

[34] H. Paik, D. I. Schuster, L. S. Bishop, G. Kirchmair, G. Catelani, A. P. Sears, B. R. Johnson, M. J. Reagor, L. Frunzio, L. I. Glazman, S. M. Girvin, M. H. Devoret, and R. J. Schoelkopf. *Observation of High Coherence in Josephson Junction Qubits Measured in a Three-Dimensional Circuit QED Architecture*. Physical Review Letters **107**(24), 240501 (2011). URL https://link.aps.org/doi/10.1103/PhysRevLett.107.240501.

[35] C. Rigetti, J. M. Gambetta, S. Poletto, B. L. T. Plourde, J. M. Chow, A. D. Córcoles, J. A. Smolin, S. T. Merkel, J. R. Rozen, G. A. Keefe, M. B. Rothwell, M. B. Ketchen, and M. Steffen. *Superconducting qubit in a waveguide cavity with a coherence time approaching 0.1 ms*. Physical Review B **86**(10), 100506 (2012). URL https://link.aps.org/doi/10.1103/PhysRevB.86.100506.

[36] C. Wen. *Coplanar Waveguide: A Surface Strip Transmission Line Suitable for Nonreciprocal Gyromagnetic Device Applications*. IEEE Transactions on Microwave Theory and Techniques **17**(12), 1087 (1969). URL http://ieeexplore.ieee.org/document/1127105/.

[37] J. Koch, T. M. Yu, J. Gambetta, A. A. Houck, D. I. Schuster, J. Majer, A. Blais, M. H. Devoret, S. M. Girvin, and R. J. Schoelkopf. *Charge-insensitive qubit design derived from the Cooper pair box*. Physical Review A **76**(4), 042319 (2007). URL https://link.aps.org/doi/10.1103/PhysRevA.76.042319.

[38] N. G. Ebensperger, B. Ferdinand, D. Koelle, R. Kleiner, M. Dressel, and M. Scheffler. *Characterizing dielectric properties of ultra-thin films using superconducting coplanar microwave resonators*. Review of Scientific Instruments **90**(11), 114701 (2019). URL http://aip.scitation.org/doi/10.1063/1.5116904.

[39] L. Wendel, V. T. Engl, G. Untereiner, N. G. Ebensperger, M. Dressel, A. Farag, M. Ubl, H. Giessen, and M. Scheffler. *Microwave probing of bulk dielectrics using superconducting coplanar resonators in distant-flip-chip geometry*. Review of Scientific Instruments **91**(5), 054702 (2020). URL http://aip.scitation.org/doi/10.1063/1.5139986.

[40] C. T. Earnest, J. H. Béjanin, T. G. McConkey, E. A. Peters, A. Korinek, H. Yuan, and M. Mariantoni. *Substrate surface engineering for high-quality silicon/aluminum superconducting resonators*. Superconductor Science and Technology **31**(12), 125013 (2018). URL https://iopscience.iop.org/article/10.1088/1361-6668/aae548.

[41] J. Gao, J. Zmuidzinas, B. A. Mazin, H. G. LeDuc, and P. K. Day. *Noise properties of superconducting coplanar waveguide microwave resonators*. Applied Physics Letters **90**(10), 102507 (2007). URL http://aip.scitation.org/doi/10.1063/1.2711770.

[42] C. R. H. McRae, J. H. Béjanin, C. T. Earnest, T. G. McConkey, J. R. Rinehart, C. Deimert, J. P. Thomas, Z. R. Wasilewski, and M. Mariantoni. *Thin film metrology and microwave loss characterization of indium and aluminum/indium superconducting planar resonators*. Journal of Applied Physics **123**(20), 205304 (2018). URL http://aip.scitation.org/doi/10.1063/1.5020514.

[43] J. Gao, M. Daal, A. Vayonakis, S. Kumar, J. Zmuidzinas, B. Sadoulet, B. A. Mazin, P. K. Day, and H. G. Leduc. *Experimental evidence for a surface distribution of two-level systems in superconducting lithographed microwave resonators*. Applied Physics Letters **92**(15), 152505 (2008). URL http://aip.scitation.org/doi/10.1063/1.2906373.

[44] W. Woods, G. Calusine, A. Melville, A. Sevi, E. Golden, D. Kim, D. Rosenberg, J. Yoder, and W. Oliver. *Determining Interface Dielectric Losses in Superconducting Coplanar-Waveguide Resonators*. Physical Review Applied **12**(1), 014012 (2019). URL https://link.aps.org/doi/10.1103/PhysRevApplied.12.014012.

[45] C. J. K. Richardson, N. P. Siwak, J. Hackley, Z. K. Keane, J. E. Robinson, B. Arey, I. Arslan, and B. S. Palmer. *Fabrication artifacts and parallel loss channels in metamorphic epitaxial aluminum superconducting resonators*. Superconductor Science and Technology **29**(6), 064003 (2016). URL https://iopscience.iop.org/article/10.1088/0953-2048/29/6/064003.

[46] J. M. Sage, V. Bolkhovsky, W. D. Oliver, B. Turek, and P. B. Welander. *Study of loss in superconducting coplanar waveguide resonators*. Journal of Applied Physics **109**(6), 063915 (2011). URL http://aip.scitation.org/doi/10.1063/1.3552890.

[47] H. Wang, M. Hofheinz, J. Wenner, M. Ansmann, R. C. Bialczak, M. Lenander, E. Lucero, M. Neeley, A. D. O'Connell, D. Sank, M. Weides, A. N. Cleland, and J. M. Martinis. *Improving the coherence time of superconducting coplanar resonators*. Applied Physics Letters **95**(23), 233508 (2009). URL http://aip.scitation.org/doi/10.1063/1.3273372.

[48] A. Bruno, G. de Lange, S. Asaad, K. L. van der Enden, N. K. Langford, and L. DiCarlo. *Reducing intrinsic loss in superconducting resonators by surface treatment and deep etching of silicon substrates*. Applied Physics Letters **106**(18), 182601 (2015). URL http://aip.scitation.org/doi/10.1063/1.4919761.

[49] J. M. Martinis and A. Megrant. *UCSB final report for the CSQ program: Review of decoherence and materials physics for superconducting qubits* p. 10.

[50] A. P. M. Place, L. V. H. Rodgers, P. Mundada, B. M. Smitham, M. Fitzpatrick, Z. Leng, A. Premkumar, J. Bryon, S. Sussman, G. Cheng, T. Madhavan, H. K. Babla, B. Jaeck, A. Gyenis, N. Yao, R. J. Cava, N. P. de Leon, and A. A. Houck. *New material platform for superconducting transmon qubits with coherence times exceeding 0.3 milliseconds*. arXiv:2003.00024 [cond-mat, physics:physics, physics:quant-ph] (2020). 2003.00024, URL http://arxiv.org/abs/2003.00024.

[51] D. S. Wisbey, J. Gao, M. R. Vissers, F. C. S. da Silva, J. S. Kline, L. Vale, and D. P. Pappas. *Effect of metal/substrate interfaces on radio-frequency loss in superconducting coplanar waveguides*. Journal of Applied Physics **108**(9), 093918 (2010). URL http://aip.scitation.org/doi/10.1063/1.3499608.

[52] A. Dunsworth, A. Megrant, C. Quintana, Z. Chen, R. Barends, B. Burkett, B. Foxen, Y. Chen, B. Chiaro, A. Fowler, R. Graff, E. Jeffrey, J. Kelly, E. Lucero, J. Y. Mutus, M. Neeley, C. Neill, P. Roushan, D. Sank, A. Vainsencher, J. Wenner, T. C. White, and J. M. Martinis. *Characterization and Reduction of Capacitive Loss Induced by Sub-Micron Josephson Junction Fabrication in Superconducting Qubits*. Applied Physics Letters **111**(2), 022601 (2017). 1706.00879, URL http://arxiv.org/abs/1706.00879.

[53] A. Megrant, C. Neill, R. Barends, B. Chiaro, Y. Chen, L. Feigl, J. Kelly, E. Lucero, M. Mariantoni, P. J. J. O'Malley, D. Sank, A. Vainsencher, J. Wenner, T. C. White, Y. Yin, J. Zhao, C. J. Palmstrøm, J. M. Martinis, and A. N. Cleland. *Planar superconducting resonators with internal quality factors above one million*. Applied Physics Letters **100**(11), 113510 (2012). URL http://aip.scitation.org/doi/10.1063/1.3693409.

[54] G. Calusine, A. Melville, W. Woods, R. Das, C. Stull, V. Bolkhovsky, D. Braje, D. Hover, D. K. Kim, X. Miloshi, D. Rosenberg, A. Sevi, J. L. Yoder, E. Dauler, and W. D. Oliver. *Analysis and mitigation of interface losses in trenched superconducting coplanar waveguide resonators*. Applied Physics Letters **112**(6), 062601 (2018). URL http://aip.scitation.org/doi/10.1063/1.5006888.

[55] D. J. Michalak, S. R. Amy, D. Aureau, M. Dai, A. Estève, and Y. J. Chabal. *Nanopatterning Si(111) surfaces as a selective surface-chemistry route*. Nature Materials **9**(3), 266 (2010). URL http://www.nature.com/articles/nmat2611.

[56] N. E. Grant, A. I. Pointon, R. Jefferies, D. Hiller, Y. Han, R. Beanland, M. Walker, and J. D. Murphy. *Atomic level termination for passivation and functionalisation of silicon surfaces*. Nanoscale **12**(33), 17332 (2020). URL http://xlink.rsc.org/?DOI=D0NR03860A.

[57] M. Yoshimoto, T. Maeda, T. Ohnishi, H. Koinuma, O. Ishiyama, M. Shinohara, M. Kubo, R. Miura, and A. Miyamoto. *Atomic-scale formation of ultrasmooth surfaces*

on sapphire substrates for high-quality thin-film fabrication. Applied Physics Letters **67**(18), 2615 (1995). URL http://aip.scitation.org/doi/10.1063/1.114313.

[58] A. Kamal, J. L. Yoder, F. Yan, T. J. Gudmundsen, D. Hover, A. P. Sears, P. Welander, T. P. Orlando, S. Gustavsson, and W. D. Oliver. *Improved superconducting qubit coherence with high-temperature substrate annealing.* arXiv:1606.09262 [cond-mat] (2016). 1606.09262, URL http://arxiv.org/abs/1606.09262.

[59] B. Qi, B. Agnarsson, K. Jonsson, S. Olafsson, and H. P. Gislason. *Characterisation of high-temperature annealing effects on α— Al $_2$ O $_3$ (0001) substrates.* Journal of Physics: Conference Series **100**(4), 042020 (2008). URL https://iopscience.iop.org/article/10.1088/1742-6596/100/4/042020.

[60] D. Zhang, Y. Wang, and Y. Gan. *Characterization of critically cleaned sapphire single-crystal substrates by atomic force microscopy, XPS and contact angle measurements.* Applied Surface Science **274**, 405 (2013). URL https://linkinghub.elsevier.com/retrieve/pii/S0169433212023082.

[61] M. Köpke and J. Weis. *Superconducting Pb as material for coplanar waveguide resonators on GaAs substrates.* Physica C: Superconductivity and its Applications **506**, 143 (2014). URL https://linkinghub.elsevier.com/retrieve/pii/S0921453414001877.

[62] F. Marsili, A. Gaggero, L. H. Li, A. Surrente, R. Leoni, F. Lévy, and A. Fiore. *High quality superconducting NbN thin films on GaAs.* Superconductor Science and Technology **22**(9), 095013 (2009). URL https://iopscience.iop.org/article/10.1088/0953-2048/22/9/095013.

[63] C. Thomas, R. E. Diaz, J. H. Dycus, M. E. Salmon, R. E. Daniel, T. Wang, G. C. Gardner, and M. J. Manfra. *Toward durable Al-InSb hybrid heterostructures via epitaxy of 2ML interfacial InAs screening layers.* Physical Review Materials **3**(12), 124202 (2019). URL https://link.aps.org/doi/10.1103/PhysRevMaterials.3.124202.

[64] J. M. Hornibrook, E. E. Mitchell, and D. J. Reilly. *Suppressing Dissipative Paths in Superconducting Coplanar Waveguide Resonators.* IEEE Transactions on Applied Superconductivity **23**(3), 1501604 (2013). URL http://ieeexplore.ieee.org/document/6473832/.

[65] M. Arzeo, F. Lombardi, and T. Bauch. *Microwave losses in MgO, LaAlO $_3$, and (La $_{0.3}$ Sr $_{0.7}$)(Al $_{0.65}$ Ta $_{0.35}$)O $_3$ dielectrics at low power and in the millikelvin temperature range.* Applied Physics Letters **104**(21), 212601 (2014). URL http://aip.scitation.org/doi/10.1063/1.4880357.

[66] S. Miki, M. Fujiwara, M. Sasaki, B. Baek, A. J. Miller, R. H. Hadfield, S. W. Nam, and Z. Wang. *Large sensitive-area NbN nanowire superconducting single-photon detectors fabricated on single-crystal MgO substrates.* Applied Physics Letters **92**(6), 061116 (2008). URL http://aip.scitation.org/doi/10.1063/1.2870099.

[67] J. Deng, K. Dong, P. Yang, Y. Peng, G. Ju, J. Hu, G. M. Chow, and J. Chen. *Large lattice mismatch effects on the epitaxial growth and magnetic properties of FePt films*. Journal of Magnetism and Magnetic Materials **446**, 125 (2018). URL https://linkinghub.elsevier.com/retrieve/pii/S0304885317324204.

[68] I. M. Dildar, M. Neklyudova, Q. Xu, H. W. Zandbergen, S. Harkema, D. Boltje, and J. Aarts. *Growing LaAlO 3 /SrTiO 3 interfaces by sputter deposition*. AIP Advances **5**(6), 067156 (2015). URL http://aip.scitation.org/doi/10.1063/1.4923285.

[69] O. Padmaraj, M. Venkateswarlu, and N. Satyanarayana. *Structural, electrical and dielectric properties of spinel type MgAl2O4 nanocrystalline ceramic particles synthesized by the gel-combustion method*. Ceramics International **41**(2), 3178 (2015). URL https://linkinghub.elsevier.com/retrieve/pii/S0272884214017210.

[70] Q.-Y. Shao, A.-D. Li, J.-B. Cheng, H.-Q. Ling, D. Wu, Z.-G. Liu, Y.-J. Bao, M. Wang, N.-B. Ming, C. Wang, H.-W. Zhou, and B.-Y. Nguyen. *Growth behavior of high k LaAlO 3 films on Si by metalorganic chemical vapor deposition for alternative gate dielectric application*. Applied Surface Science **250**(1-4), 14 (2005). URL https://linkinghub.elsevier.com/retrieve/pii/S0169433204018379.

[71] S. V. Egorov, A. A. Sorokin, I. E. Ilyakov, B. V. Shishkin, E. A. Serov, V. V. Parshin, K. I. Rybakov, S. S. Balabanov, and A. V. Belyaev. *Terahertz Dielectric Properties of Polycrystalline MgAl2O4 Spinel Obtained by Microwave Sintering and Hot Pressing*. Journal of Infrared, Millimeter, and Terahertz Waves **40**(4), 447 (2019). URL http://link.springer.com/10.1007/s10762-019-00582-4.

[72] R. Shannon and G. Rossman. *Dielectric constant of MgAl2O4 spinel and the oxide additivity rule*. Journal of Physics and Chemistry of Solids **52**(9), 1055 (1991). URL https://linkinghub.elsevier.com/retrieve/pii/0022369791900382.

[73] G. Benz, T. Scherer, M. Neuhaus, and W. Jutzi. *Quality factors of coplanar niobium resonators on LaAlO3 substrates with different cross-sectional geometries*. Cryogenics **38**(6), 697 (1998). URL https://linkinghub.elsevier.com/retrieve/pii/S0011227598000472.

[74] A. S. Cooper. *Precise lattice constants of germanium, aluminum, gallium arsenide, uranium, sulphur, quartz and sapphire*. Acta Crystallographica **15**(6), 578 (1962). URL http://scripts.iucr.org/cgi-bin/paper?S0365110X62001474.

[75] Y.-L. Han, S.-C. Shen, J. You, H.-O. Li, Z.-Z. Luo, C.-J. Li, G.-L. Qu, C.-M. Xiong, R.-F. Dou, L. He, D. Naugle, G.-P. Guo, and J.-C. Nie. *Two-dimensional superconductivity at (110) LaAlO 3 /SrTiO 3 interfaces*. Applied Physics Letters **105**(19), 192603 (2014). URL http://aip.scitation.org/doi/10.1063/1.4901940.

[76] S. Gariglio, M. Gabay, and J.-M. Triscone. *Research Update: Conductivity and beyond at the LaAlO 3 /SrTiO 3 interface*. APL Materials **4**(6), 060701 (2016). URL http://aip.scitation.org/doi/10.1063/1.4953822.

[77] H. Noad, P. Wittlich, J. Mannhart, and K. A. Moler. *Modulation of Superconducting Transition Temperature in LaAlO3/SrTiO3 by SrTiO3 Structural Domains*. Journal of Superconductivity and Novel Magnetism **32**(4), 821 (2019). URL http://link.springer.com/10.1007/s10948-018-4730-8.

[78] M. R. Vissers, J. Gao, D. S. Wisbey, D. A. Hite, C. C. Tsuei, A. D. Corcoles, M. Steffen, and D. P. Pappas. *Low loss superconducting titanium nitride coplanar waveguide resonators*. Applied Physics Letters **97**(23), 232509 (2010). URL http://aip.scitation.org/doi/10.1063/1.3517252.

[79] J. M. Gambetta, C. E. Murray, Y.-K.-K. Fung, D. T. McClure, O. Dial, W. Shanks, J. W. Sleight, and M. Steffen. *Investigating Surface Loss Effects in Superconducting Transmon Qubits*. IEEE Transactions on Applied Superconductivity **27**(1), 1 (2017). URL http://ieeexplore.ieee.org/document/7745914/.

[80] J. C. Maxwell. *VIII. A dynamical theory of the electromagnetic field*. Philosophical Transactions of the Royal Society of London **155**, 459 (1865). URL https://royalsocietypublishing.org/doi/10.1098/rstl.1865.0008.

[81] M. Dressel and G. Grüner. *Electrodynamics of Solids: Optical Properties of Electrons in Matter* (Cambridge University Press, 2002), first ed. URL https://www.cambridge.org/core/product/identifier/9780511606168/type/book.

[82] J. Bardeen, L. N. Cooper, and J. R. Schrieffer. *Theory of Superconductivity*. Physical Review **108**(5), 1175 (1957). URL https://link.aps.org/doi/10.1103/PhysRev.108.1175.

[83] M. Göppl, A. Fragner, M. Baur, R. Bianchetti, S. Filipp, J. M. Fink, P. J. Leek, G. Puebla, L. Steffen, and A. Wallraff. *Coplanar waveguide resonators for circuit quantum electrodynamics*. Journal of Applied Physics **104**(11), 113904 (2008). URL http://aip.scitation.org/doi/10.1063/1.3010859.

[84] P. Esquinazi, ed. *Tunneling Systems in Amorphous and Crystalline Solids* (Springer-Verlag, Berlin Heidelberg, 1998). URL https://www.springer.com/gp/book/9783540639602.

[85] R. B. Goldfarb. *The Permeability of Vacuum and the Revised International System of Units*. IEEE Magnetics Letters **8**, 1 (2017). URL https://ieeexplore.ieee.org/document/8241772/.

[86] M. Naghiloo. *Introduction to Experimental Quantum Measurement with Superconducting Qubits*. arXiv:1904.09291 [quant-ph] (2019). 1904.09291, URL http://arxiv.org/abs/1904.09291.

[87] D. Pozar. *Microwave Engineering, 4th Edition* (Wiley, 2011). URL https://books.google.com.au/books?id=JegbAAAAQBAJ.

[88] W. Meissner and R. Ochsenfeld. *Ein neuer effekt bei eintritt der supraleitfähigkeit.* Naturwissenschaften **21**(44), 787 (1933).

[89] F. London, H. London, and F. A. Lindemann. *The electromagnetic equations of the supraconductor.* Proceedings of the Royal Society of London. Series A - Mathematical and Physical Sciences **149**(866), 71 (1935). URL https://royalsocietypublishing.org/doi/abs/10.1098/rspa.1935.0048.

[90] P. Mangin and R. Kahn. *Superconductivity* (Springer International Publishing, Cham, 2017). URL http://link.springer.com/10.1007/978-3-319-50527-5.

[91] R. Barends. *Photon-Detecting Superconducting Resonators.* Ph.D. thesis, R. Barends (2009). URL https://repository.tudelft.nl/islandora/object/uuid%3A574944e6-c3ce-4c86-a511-a88385b22379.

[92] M. S. Khalil, M. J. A. Stoutimore, F. C. Wellstood, and K. D. Osborn. *An analysis method for asymmetric resonator transmission applied to superconducting devices.* Journal of Applied Physics **111**(5), 054510 (2012). URL http://aip.scitation.org/doi/10.1063/1.3692073.

[93] M. Scigliuzzo, L. E. Bruhat, A. Bengtsson, J. J. Burnett, A. F. Roudsari, and P. Delsing. *Phononic loss in superconducting resonators on piezoelectric substrates.* New Journal of Physics **22**(5), 053027 (2020). URL https://iopscience.iop.org/article/10.1088/1367-2630/ab8044.

[94] P. J. Petersan and S. M. Anlage. *Measurement of resonant frequency and quality factor of microwave resonators: Comparison of methods.* Journal of Applied Physics **84**(6), 3392 (1998). URL http://aip.scitation.org/doi/10.1063/1.368498.

[95] J. Gao. *The Physics of Superconducting Microwave Resonators.* Ph.D. thesis, California Institute of Technology, (2008).

[96] M. Sandberg, M. R. Vissers, J. S. Kline, M. Weides, J. Gao, D. S. Wisbey, and D. P. Pappas. *Etch induced microwave losses in titanium nitride superconducting resonators.* Applied Physics Letters **100**(26), 262605 (2012). URL http://aip.scitation.org/doi/10.1063/1.4729623.

[97] Y. Shalibo, Y. Rofe, D. Shwa, F. Zeides, M. Neeley, J. M. Martinis, and N. Katz. *Lifetime and Coherence of Two-Level Defects in a Josephson Junction.* Physical Review Letters **105**(17), 177001 (2010). URL https://link.aps.org/doi/10.1103/PhysRevLett.105.177001.

[98] C. Müller, A. Shnirman, and Y. Makhlin. *Relaxation of Josephson qubits due to strong coupling to two-level systems.* Physical Review B **80**(13), 134517 (2009). URL https://link.aps.org/doi/10.1103/PhysRevB.80.134517.

[99] J. Lisenfeld, G. J. Grabovskij, C. Müller, J. H. Cole, G. Weiss, and A. V. Ustinov. *Observation of directly interacting coherent two-level systems in an amorphous material.* Nature Communications **6**(1), 6182 (2015). URL http://www.nature.com/articles/ncomms7182.

[100] P. Dutta and P. M. Horn. *Low-frequency fluctuations in solids: 1 f noise.* Reviews of Modern Physics **53**(3), 497 (1981). URL https://link.aps.org/doi/10.1103/RevModPhys.53.497.

[101] C. M. Quintana, Y. Chen, D. Sank, A. G. Petukhov, T. C. White, D. Kafri, B. Chiaro, A. Megrant, R. Barends, B. Campbell, Z. Chen, A. Dunsworth, A. G. Fowler, R. Graff, E. Jeffrey, J. Kelly, E. Lucero, J. Y. Mutus, M. Neeley, C. Neill, V. N. Smelyanskiy, A. Vainsencher, J. Wenner, H. Neven, and J. M. Martinis. *Observation of Classical-Quantum Crossover of 1=f Flux Noise and Its Paramagnetic Temperature Dependence.* Physical Review Letters p. 6 (2017).

[102] R. Barends, J. Baselmans, J. Hovenier, J. Gao, S. Yates, T. Klapwijk, and H. Hoevers. *Niobium and Tantalum High Q Resonators for Photon Detectors.* IEEE Transactions on Applied Superconductivity **17**(2), 263 (2007). URL http://ieeexplore.ieee.org/document/4277287/.

[103] B. T. Matthias, T. H. Geballe, and V. B. Compton. *Superconductivity.* Reviews of Modern Physics **35**(1), 1 (1963). URL https://link.aps.org/doi/10.1103/RevModPhys.35.1.

[104] D. I. Schuster. *Circuit Quantum Electrodynamics.* Ph.D. thesis, Yale (2007).

[105] L. Childress, A. S. Sørensen, and M. D. Lukin. *Mesoscopic cavity quantum electrodynamics with quantum dots.* Physical Review A **69**(4), 042302 (2004). URL https://link.aps.org/doi/10.1103/PhysRevA.69.042302.

[106] H. M. I. Jaim, J. A. Aguilar, B. Sarabi, Y. J. Rosen, A. N. Ramanayaka, E. H. Lock, C. J. K. Richardson, and K. D. Osborn. *Superconducting TiN Films Sputtered Over a Large Range of Substrate DC Bias.* IEEE Transactions on Applied Superconductivity **25**(3), 1 (2015). URL http://ieeexplore.ieee.org/document/6942188/.

[107] E. H. Lock, P. Xu, T. Kohler, L. Camacho, J. Prestigiacomo, Y. J. Rosen, and K. D. Osborn. *Using Surface Engineering to Modulate Superconducting Coplanar Microwave Resonator Performance.* IEEE Transactions on Applied Superconductivity **29**(6), 1 (2019). URL https://ieeexplore.ieee.org/document/8606149/.

[108] J. R. Kim, J. N. Lee, J. Mun, Y. Kim, Y. J. Shin, B. Kim, S. Das, L. Wang, M. Kim, M. Lippmaa, T. H. Kim, and T. W. Noh. *Experimental realization of atomically flat and Al O 2 -terminated LaAl O 3 (001) substrate surfaces.* Physical Review Materials **3**(2), 023801 (2019). URL https://link.aps.org/doi/10.1103/PhysRevMaterials.3.023801.

[109] R. T. Haasch, E. Breckenfeld, and L. W. Martin. *Single Crystal Perovskites Analyzed Using X-ray Photoelectron Spectroscopy: 3. LaAlO ₃ (001).* Surface Science Spectra **21**(1), 103 (2014). URL http://avs.scitation.org/doi/10.1116/11.20140903.

[110] G. Dold, C. W. Zollitsch, J. O'Sullivan, S. Welinski, A. Ferrier, P. Goldner, S. de Graaf, T. Lindström, and J. J. Morton. *High-Cooperativity Coupling of a Rare-Earth Spin Ensemble to a Superconducting Resonator Using Yttrium Orthosilicate as a Substrate.* Physical Review Applied **11**(5), 054082 (2019). URL https://link.aps.org/doi/10.1103/PhysRevApplied.11.054082.

[111] A. Nersisyan, E. A. Sete, S. Stanwyck, A. Bestwick, M. Reagor, S. Poletto, N. Alidoust, R. Manenti, R. Renzas, C.-V. Bui, K. Vu, T. Whyland, and Y. Mohan. *Manufacturing low dissipation superconducting quantum processors.* In *2019 IEEE International Electron Devices Meeting (IEDM)*, pp. 31.1.1–31.1.4 (IEEE, San Francisco, CA, USA, 2019). URL https://ieeexplore.ieee.org/document/8993458/.

[112] G. L. Weibel and C. K. Ober. *An overview of supercritical CO2 applications in microelectronics processing.* Microelectronic Engineering **65**(1-2), 145 (2003). URL https://linkinghub.elsevier.com/retrieve/pii/S0167931702007475.

[113] C. Wang, C. Axline, Y. Y. Gao, T. Brecht, Y. Chu, L. Frunzio, M. H. Devoret, and R. J. Schoelkopf. *Surface participation and dielectric loss in superconducting qubits.* Applied Physics Letters **107**(16), 162601 (2015). URL http://aip.scitation.org/doi/10.1063/1.4934486.

[114] G. Binnig, C. F. Quate, and C. Gerber. *Atomic Force Microscope.* Physical Review Letters **56**(9), 930 (1986). URL https://link.aps.org/doi/10.1103/PhysRevLett.56.930.

[115] G. Meyer and N. M. Amer. *Novel optical approach to atomic force microscopy.* Applied Physics Letters **53**(12), 1045 (1988). URL http://aip.scitation.org/doi/10.1063/1.100061.

[116] F. J. Giessibl. *Advances in atomic force microscopy.* Rev. Mod. Phys. **75**(3), 35 (2003).

[117] E. Abbe. *Beiträge zur Theorie des Mikroskops und der mikroskopischen Wahrnehmung.* Archiv für Mikroskopische Anatomie **9**(1), 413 (1873). URL http://link.springer.com/10.1007/BF02956173.

[118] J. E. Sader and S. P. Jarvis. *Coupling of conservative and dissipative forces in frequency-modulation atomic force microscopy.* Physical Review B **74**(19), 195424 (2006). URL https://link.aps.org/doi/10.1103/PhysRevB.74.195424.

[119] J. E. Sader and S. P. Jarvis. *Interpretation of frequency modulation atomic force microscopy in terms of fractional calculus.* Physical Review B **70**(1), 012303 (2004). URL https://link.aps.org/doi/10.1103/PhysRevB.70.012303.

[120] D. Nečas, M. Valtr, and P. Klapetek. *How levelling and scan line corrections ruin roughness measurement and how to prevent it*. Scientific Reports **10**(1), 15294 (2020). URL http://www.nature.com/articles/s41598-020-72171-8.

[121] J. Moulder and J. Chastain. *Handbook of X-Ray Photoelectron Spectroscopy: A Reference Book of Standard Spectra for Identification and Interpretation of XPS Data* (Physical Electronics Division, Perkin-Elmer Corporation, 1992). URL https://books.google.com.au/books?id=A_XGQgAACAAJ.

[122] *CMM: Kratos Axis Ultra XPS* (2016). URL https://cmm.centre.uq.edu.au/xps.

[123] P. p. jacobson@uni-graz at)Jacobson. *Lectures on Structure and Matter* (2017).

[124] H. Kiessig. *Interferenz von Röntgenstrahlen an dünnen Schichten*. Annalen der Physik **402**(7), 769 (1931). URL http://doi.wiley.com/10.1002/andp.19314020702.

[125] O. S. Heavens. *Optical properties of thin films*. Reports on Progress in Physics **23**(1), 1 (1960). URL https://doi.org/10.1088/0034-4885/23/1/301.

[126] L. Névot and P. Croce. *Caractérisation des surfaces par réflexion rasante de rayons X. Application à l'étude du polissage de quelques verres silicates*. Revue de Physique Appliquée **15**(3), 761 (1980). URL http://www.edpsciences.org/10.1051/rphysap:01980001503076100.

[127] A. Nelson. *Motofit* (2007). URL http://motofit.sourceforge.net.

[128] R. Gunnarsson, A. Kalabukhov, and D. Winkler. *Evaluation of recipes for obtaining single terminated perovskite oxide substrates*. Surface Science **603**(1), 151 (2009). URL https://linkinghub.elsevier.com/retrieve/pii/S0039602808007681.

[129] T. N. Jensen, M. K. Rasmussen, J. Knudsen, A. Vlad, S. Volkov, E. Lundgren, A. Stierle, and J. V. Lauritsen. *Correlation between stoichiometry and surface structure of the polar $MgAl_2O_4$ (100) surface as a function of annealing temperature*. Physical Chemistry Chemical Physics **17**(8), 5795 (2015). URL http://xlink.rsc.org/?DOI=C4CP05878J.

[130] K. Bordo and H.-G. Rubahn. *Effect of Deposition Rate on Structure and Surface Morphology of Thin Evaporated Al Films on Dielectrics and Semiconductors*. Materials Science **18**(4), 313 (2012). URL http://www.matsc.ktu.lt/index.php/MatSc/article/view/3088.

[131] K. Seeger. *Microwave dielectric constants of silicon, gallium arsenide, and quartz*. Journal of Applied Physics **63**(11), 5439 (1988). URL http://aip.scitation.org/doi/10.1063/1.341153.

[132] P. Rai-Choudhury. *Handbook of Microlithography, Micromachining, and Microfabrication. Volume 1: Microlithography* (SPIE PRESS, 1997). URL http://ebooks.spiedigitallibrary.org/book.aspx?doi=10.1117/3.2265070.

[133] *Technical data sheet: AZ 1500 series standard photoresist.* URL https://www.microchemicals.com/micro/tds_az_1500_series.pdf.

[134] W. Schumann. *Gemstones of the World, Revised Edition* (Sterling, New York, 2000), revised, subsequent edition ed.

[135] G. V. Samsonov. *Mechanical Properties of the Elements.* In G. V. Samsonov, ed., *Handbook of the Physicochemical Properties of the Elements*, pp. 387–446 (Springer US, Boston, MA, 1968). URL https://doi.org/10.1007/978-1-4684-6066-7_7.

[136] *MSE Supplies LLC: MgAl2O4 Magnesium Aluminate (Spinel) Crystal Substrates.* URL https://www.msesupplies.com/products/magnesium-aluminate-mgal2o4-crystal-substrates.

[137] *MgAl2O4 crystal (spinel): Datasheet.* URL www.mtixtl.com.

[138] *CrysTec Krystalltechnologie: LaAlO3 for Research and Development.* URL http://www.crystec.de/daten/laalo3.pdf.

[139] V. Parma. *Cryostat Design* (2014). URL http://cds.cern.ch/record/1974062.

[140] R. Barends, J. Wenner, M. Lenander, Y. Chen, R. C. Bialczak, J. Kelly, E. Lucero, P. O'Malley, M. Mariantoni, D. Sank, H. Wang, T. C. White, Y. Yin, J. Zhao, A. N. Cleland, J. M. Martinis, and J. J. A. Baselmans. *Minimizing quasiparticle generation from stray infrared light in superconducting quantum circuits.* Applied Physics Letters **99**(11), 113507 (2011). URL http://aip.scitation.org/doi/10.1063/1.3638063.

[141] S. Gustavsson, F. Yan, G. Catelani, J. Bylander, A. Kamal, J. Birenbaum, D. Hover, D. Rosenberg, G. Samach, A. P. Sears, S. J. Weber, J. L. Yoder, J. Clarke, A. J. Kerman, F. Yoshihara, Y. Nakamura, T. P. Orlando, and W. D. Oliver. *Suppressing relaxation in superconducting qubits by quasiparticle pumping.* Science **354**(6319), 1573 (2016). URL https://www.sciencemag.org/lookup/doi/10.1126/science.aah5844.

[142] D. Bothner, T. Gaber, M. Kemmler, D. Koelle, and R. Kleiner. *Improving the performance of superconducting microwave resonators in magnetic fields.* Applied Physics Letters **98**(10), 102504 (2011). URL http://aip.scitation.org/doi/10.1063/1.3560480.

[143] D. P. Pappas, M. R. Vissers, D. S. Wisbey, J. S. Kline, and J. Gao. *Two Level System Loss in Superconducting Microwave Resonators.* IEEE Transactions on Applied Superconductivity **21**(3), 871 (2011). URL http://ieeexplore.ieee.org/document/5685585/.

[144] C.-T. Wang and S.-C. Yen. *Theoretical analysis of film uniformity in spinning processes.* Chemical Engineering Science **50**(6), 989 (1995). URL https://linkinghub.elsevier.com/retrieve/pii/0009250994004816.

[145] G. Li, J. Ohta, A. Kobayashi, and H. Fujioka. *Room-temperature epitaxial growth of AlN on atomically flat MgAl2O4 substrates.* Applied Physics Letters **89**(18), 182104 (2006). URL http://aip.scitation.org/doi/10.1063/1.2372685.

[146] S. Bueble, K. Knorr, E. Brecht, and W. W. Schmahl. *Influence of the ferroelastic twin domain structure on the {100} surface morphology of LaAlO3 HTSC substrates.* Surface Science **400**(1), 345 (1998). URL https://www.sciencedirect.com/science/article/pii/S0039602897008911.

[147] C. M. Quintana, A. Megrant, Z. Chen, A. Dunsworth, B. Chiaro, R. Barends, B. Campbell, Y. Chen, I.-C. Hoi, E. Jeffrey, J. Kelly, J. Y. Mutus, P. J. J. O'Malley, C. Neill, P. Roushan, D. Sank, A. Vainsencher, J. Wenner, T. C. White, A. N. Cleland, and J. M. Martinis. *Characterization and reduction of microfabrication-induced decoherence in superconducting quantum circuits.* Applied Physics Letters **105**(6), 062601 (2014). URL http://aip.scitation.org/doi/10.1063/1.4893297.